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(c) 2009 American Mathematical Society
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Set	Items	Description
S1	37509	DIGITAL(3W)(CHANNEL??? OR PATH??? OR LINK??? OR LINE)
S2	8120	ANALOG(3W)(PATH??? OR LINK??? OR LINE OR CHANNEL??? OR CHANEL???)
S3	106309	ADC OR (ANALOG(2W)DIGITAL OR A()D)(2W)CONVER??????
S4	2401	(PLURAL? OR MANY OR MULTI OR MULTIPLE? ? OR NUMEROUS?? OR -SEVERAL? ? OR DIFFERENT?? OR TWO OR ARRAY??)(3N)(S1 OR S2)
S5	227	(SMALLER OR LOWER OR LESS???)(7N)(S1 OR S2)
S6	243	(GREATER OR HIGHER OR LARGER OR BIGGER)(7N)(S1 OR S2)

S7 321 AU=(AGAZZI O? OR AGAZZI, O? OR GOPINATHAN V? OR GAPINATHAN, V?)
S8 0 S1 AND S2 AND S3 AND S4 AND (S5 OR S6)
S9 340 S1 AND S2 AND S3
S10 2 S9 AND (S5 OR S6)
S11 1 RD (unique items)
S12 0 S10 AND S4
S13 34 S9 AND S4
S14 23 RD (unique items)
S15 20 S14 NOT PY>2000
S16 658 (COMPAR???? OR MATCH???)(7N)(S1 OR S2)
S17 10 S16 AND S1 AND S2 AND S3
S18 8 RD (unique items)
S19 2 S18 NOT PY>2000
S20 2 S7 AND S1 AND S2 AND S3

11/3,K/1 (Item 1 from file: 60)
DIALOG(R)File 60:ANTE: Abstracts in New Tech & Engineer

0000883438 IP ACCESSION NO: 2008609454
Implantable medical device with adjustable sigma-delta analog-to-digital conversion clock rate

Frigaard, Mark A; Heinks, Michael W; Anderson, Joel A; Mehregan, Robert H

, USA
PUBLISHER URL:
http://patft.uspto.gov/netacgi/nph-Parser?Sect1=PTO2&Sect2=HITOFF&u=/netahtml/PTO/search-adv.htm&r=1&p=1&f=G&l=50&d=PTXT&S1=7345607.PN.&OS=pn/7345607&RS=PN/7345607

DOCUMENT TYPE: Patent
RECORD TYPE: Abstract
LANGUAGE: English
FILE SEGMENT: ANTE: Abstracts in New Technologies and Engineering

DESCRIPTORS: Analog to digital conversion; **Channels** ; Clocks; Surgical implants; Converters; Digital signal processing; Thresholds; Battery; Pacemakers; Conversion; Power consumption; Signal detection...

15/3,K/1 (Item 1 from file: 8)
DIALOG(R)File 8:Ei Compendex(R)

0013747254 E.I. COMPENDEX No: 1997020413646
Digital filtering of multiple analog channels
Hicks, William T.
Corresp. Author/Affil: Hicks, William T.
Conference Title: Proceedings of the 1996 International Telemetering Conference, ITC
Conference Location: San Diego, CA, USA Conference Date: 19961028-19961031
E.I. Conference No.: 45601
International Telemetering Conference (Proceedings) (Int Telem Conf Proc) 1996, 32/- (225-232)
Publication Date: 19961201
Publisher: Instrument Society of America
CODEN: ITCOD ISSN: 0884-5123
Document Type: Conference Paper; Conference Proceeding Record Type: Abstract
Treatment: A; (Applications); X; (Experimental)
Language: English Summary Language: English
Number of References: 2

Digital filtering of multiple analog channels
Descriptors: **Analog** to **digital conversion** ; Anti-aliasing; Digital filters; Frequencies; Performance; Pulse code modulation; Telemetering; *Digital signal processing
Identifiers: Cutoff frequencies; **Digital** filtering; **Multiple analog channels** ; Signal conditioning

15/3,K/2 (Item 2 from file: 8)
DIALOG(R)File 8:Ei Compendex(R)

0013244031 E.I. COMPENDEX No: 1994111411033
Analysis of clipping effect in DMT-based ADSL systems
Mestdagh, Denis J.G.; Spruyt, Paul; Biran, Bernard
Corresp. Author/Affil: Mestdagh, Denis J.G.: Alcatel-Bell, Antwerp, Belgium
Conference Title: Proceedings of the 1994 IEEE International Conference on Communications
Conference Location: New Orleans, LA, USA Conference Date: 19940501-19940505
E.I. Conference No.: 20804
Conference Record - International Conference on Communications (Conf Rec Int Conf Commun) 1994, 1/- (293-300)
Publication Date: 19940101
Publisher: Publ by IEEE
CODEN: CICCD ISSN: 0536-1486 ISBN: 0780318269; 9780780318267
Document Type: Conference Paper; Conference Proceeding Record Type: Abstract
Treatment: T; (Theoretical)

Language: English Summary Language: English
Number of References: 11
...By combining this expression with the well-known expression for the quantization noise in the **A / D** -D/A **converters** , it is shown how clipping can reduce the number of bits of **A / D** -D/A **converters** as well as the dynamical range of the line drivers while keeping the overall SNR...
Descriptors: Amplitude modulation; **Analog** to **digital conversion** ; Carrier communication; **Channel** capacity; Communication channels (information theory); Digital communication systems; Digital signal processing; Digital to analog conversion...
Identifiers: AD/DA converters; Constellation; Conventional **analog** voice **channel** ; Discrete **multi** tone; Power spectrum; Quadrature amplitude modulation

15/3,K/3 (Item 3 from file: 8)
DIALOG(R)File 8:Ei Compendex(R)

0012389615 E.I. COMPENDEX No: 1990070016138
CAMAC-compatible microprocessor controller with analog-to- digital **-to-** analog channel
Tsymbalenko, V.L.
Corresp. Author/Affil: Tsymbalenko, V.L.
Instruments and experimental techniques New York (Instrum Exp Tech) 1989, 31/5 pt 1 (1177-1179)
Publication Date: 19891201
CODEN: INETA ISSN: 0020-4412
Document Type: Article; Journal Record Type: Abstract
Treatment: X; (Experimental)
Language: English Summary Language: English
Number of References: 6

CAMAC-compatible microprocessor controller with analog-to- digital **-to-** analog channel
...contains a central processor, 2K of ROM, 2K of RAM, an eight-channel 12-bit **analog - digital converter** (0-10 V and (approximate)30 musec), **two** 12-bit **digital - analog channels** , a 24-bit parallel input/output port, a timer, and an asynchronous parallel CAMAC interface...
Descriptors: Computer Interfaces; Data Conversion, **Analog** to **Digital** ; Data **Conversion** , Digital to Analog; Electronic Circuits, Flip Flop; Integrated Circuits; *Control Equipment

15/3,K/4 (Item 4 from file: 8)
DIALOG(R)File 8:Ei Compendex(R)

05979642 E.I. COMPENDEX No: 19590017007
Inst Radio Engrs -- 2nd Nat Convention on military electronics
Anon(Ed.)
Conference Title: Institute of Radio Engineers -- Conference Proceedings of the 2nd National Convention on Military Electronics
Conference Location: Washington, DC Conference Date: 19580616-19580618
Institute of Radio Engineers -- National Convention on Military Electronics -- Conference Proceedings 412p

Publication Year: 1958
Document Type: CP; (Conference Proceedings)
Language: English

...Analog Input, S.D. WARNER, 75-8; Use of Microwave Links for Combined Handling of **Digital** , **Analog** and **Multi - Channel** Voice Information, V.GRAZIANO, 79-83; Small, Light-Weight Traveling-Wave Tube Chain for S...

...O.OTLEY, R.F. SHOEMAKER, P.J.FRANKLIN, 310-13; Sine-Cosine Encoding Using Linear **Analog** to **Digital Converters** , E.J.S MITH, 314-17; Waveform Compander, W.F.UPLINGER, P.W.JENSEN, 318...

15/3,K/5 (Item 1 from file: 2)
DIALOG(R)File 2:INSPEC
(c) 2009 Institution of Electrical Engineers. All rts. reserv.

01433490 INSPEC Abstract Number: B72033404
Title: ORBIT: Online Reduced Bandwidth Information Transmission
Author(s): Oberbeck, P.E.R.
University: Univ. Illinois Urbana-Champaign, IL, USA
Dissertation Date: 1971
Country of Publication: USA 88 pp.
Language: English
Subfile: B C

...Abstract: black on white line drawings. The encoding and decoding of the picture are done by **two digital** processors. The transmission **link** between **two** digital processors is an **analog line** with **a D** /A **conversion** at the transmitter an **A / D conversion** at the receiver. The paper describes in detail the operation of the transmitter and receiver ...

...Identifiers: **A / D conversion** ;

15/3,K/6 (Item 1 from file: 6)
DIALOG(R)File 6:NTIS
(c) 2009 NTIS, Intl Cpyrght All Rights Res. All rts. reserv.

1390764 NTIS Accession Number: AD-A196 515/1
Microprocessor Control of a Fast Analog **-to-** Digital Converter **for an Underwater Fiber Optic Data Link**
(Master's thesi)
Schlechte, G. L.
Naval Postgraduate School, Monterey, CA.
Corp. Source Codes: 019895000; 251450
Mar 88 65p
Languages: English Document Type: Thesis
Journal Announcement: GRAI8823
Order this product from NTIS by: phone at 1-800-553-NTIS (U.S. customers); (703)605-6000 (other countries); fax at (703)321-8547; and email at orders@ntis.fedworld.gov. NTIS is located at 5285 Port Royal Road, Springfield, VA, 22161, USA.
NTIS Prices: PC A04/MF A01

Microprocessor Control of a Fast Analog **-to-** Digital Converter **for an**

Underwater Fiber Optic Data Link
The thesis reports on the design and evaluation of a microprocessor-controlled, high-speed **analog** -to- **digital converter** . The processor supervises and manages the digital conversion, split-phase encoding (Manchester) and framing of...

... ease of future system enhancements. An example would be the implementation of one package to **multiplex** several **analog channels** from a local sensor network over the single fiber optic link to the shore station. Keywords: **Analog** -to- **Digital converter** , Digital **conversion** , Split phase encoding, and Manchester. (r.h.)
Descriptors: ***Analog** to **digital converters** ; *Data **links** ; *Fiber optics; *Microprocessors; Analog systems; Coding; Detectors; Digital computers; Intelligence; Networks; Reports; Signals; Stations; Theses

15/3,K/7 (Item 2 from file: 6)
DIALOG(R)File 6:NTIS
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1381251 NTIS Accession Number: AD-A193 842/2
Multichannel Data Transmission through a Fiber Optic Cable
(Master's thesi)
Hatzidakis, F.
Naval Postgraduate School, Monterey, CA.
Corp. Source Codes: 019895000; 251450
Dec 87 92p
Languages: English Document Type: Thesis
Journal Announcement: GRAI8819
Order this product from NTIS by: phone at 1-800-553-NTIS (U.S. customers); (703)605-6000 (other countries); fax at (703)321-8547; and email at orders@ntis.fedworld.gov. NTIS is located at 5285 Port Royal Road, Springfield, VA, 22161, USA.
NTIS Prices: PC A05/MF A01

... this thesis was to design and construct a system which transmits and receives data from **different analog channels** through a single fiber optic cable link. The system uses a microprocessor controlled multiplexer and a high speed **analog** -to- **digital converter** . Tests and measurements were performed to examine the restrictions, problems and different options on the...
Descriptors: *Fiber optics transmission lines; *Multichannel communications; *Light transmission; *Optical communications; Analog systems; **Analog** to **digital converters** ; **Channels** ; Control; Data transmission systems; Microprocessors; Multiplexing; Trade off analysis; Transmitting; Theses; Registers(Circuits); Central processing...

15/3,K/8 (Item 1 from file: 144)
DIALOG(R)File 144:Pascal
(c) 2009 INIST/CNRS. All rts. reserv.

14772794 PASCAL No.: 00-0452086
Implementation of SDR-based digital IF channelizer/de-channelizer for multiple CDMA signals
IM S; LEE W; KIM C; SHIN Y; LEE S H; CHUNG J

Soongsil Univ, Seoul, Korea, Republic of
Journal: IEICE Transactions on Communications, 2000, v E83-B (6) 1282-1289
Language: English

This paper presents the results on IF/baseband up/down direct **digital** conversion and **multiple channel** analysis/synthesis software defined radio modules which are implemented using high speed **ADC** , DAC and FPGA, for IS-95 code division multiple access (CDMA) systems. The implemented system...

English Descriptors: Polyphase filter banks; Software digital radio (SDR); Wideband channelizer-dechannelizer systems; Application; Code division **multiple** access; Digital to **analog** conversion; Communication **channels** (information theory); Computer software selection and evaluation; Signal filtering and prediction; Digital radio; Reviews

15/3,K/9 (Item 1 from file: 99)
DIALOG(R)File 99:Wilson Appl. Sci & Tech Abs
(c) 2009 The HW Wilson Co. All rts. reserv.

2190559 H.W. WILSON RECORD NUMBER: BAST00064104
Multiplex large RTD sensor arrays for lower parts count
Woodward, W. Stephen;
Electronic Design v. 48 no19 (Sept. 18 2000) p. 163-4
DOCUMENT TYPE: Feature Article ISSN: 0013-4872

...ABSTRACT: it can get expensive rather quickly. The proposed multiplex circuit cuts the required number of **analog** -to- **digital converter channels** and **array** connections to reduce costs.

15/3,K/10 (Item 1 from file: 60)
DIALOG(R)File 60:ANTE: Abstracts in New Tech & Engineer
(c) 2009 CSA. All rts. reserv.

0002132203 IP ACCESSION NO: 20082113397
Direct digital synthesizer producing a signal representing an amplitude of a sine wave

Solbrig, Wayne E

, USA
PUBLISHER URL:
http://patft.uspto.gov/netacgi/nph-Parser?Sect1=PTO2&Sect2=HITOFF&u=/netahtml/PTO/search-adv.htm&r=1&p=1&f=G&l=50&d=PTXT&S1=7436166.PN.&OS=pn/7436166&RS=PN/7436166

DOCUMENT TYPE: Patent
RECORD TYPE: Abstract
LANGUAGE: English
FILE SEGMENT: ANTE: Abstracts in New Technologies and Engineering

ABSTRACT:
... and a second signal that is phase shifted relative to the first

signal. A first **analog** -to- **digital channel** processes the first signal to produce an in-phase and quadrature signals. The second signal is processed by a second **analog** -to- **digital channel** to produce a second set of in-phase and quadrature signals. The two sets of...

...the signal of the device under test and a local oscillator signal associated with the **two analog** -to- **digital channels** . The invention is further directed to a direct digital synthesizer that is capable of use ...

DESCRIPTORS: **Digital** ; Sine waves; Synthesizers; **Channels** ; Quadratures; **Analog** to **digital conversion** ; Integers; Inventions; Amplitudes; Devices; Phase detectors; Tables (data); Oscillators; Phase shifters; Mathematical analysis; Clocks; Phase...

15/3,K/11 (Item 2 from file: 60)
DIALOG(R)File 60:ANTE: Abstracts in New Tech & Engineer
(c) 2009 CSA. All rts. reserv.

0001849625 IP ACCESSION NO: 20081690316
Data processor including an A / D converter **for** converting **a** plurality **of** analog **input** channels **into digital data**

Ishimoto, Satomi; Matsushima, Osamu; Sakuma, Hajime

, USA
PUBLISHER URL:
http://patft.uspto.gov/netacgi/nph-Parser?Sect1=PTO2&Sect2=HITOFF&u=/netahtml/PTO/search-adv.htm&r=1&p=1&f=G&l=50&d=PTXT&S1=4996639.PN.&OS=pn/4996639&RS=PN/4996639

DOCUMENT TYPE: Patent
RECORD TYPE: Abstract
LANGUAGE: English
FILE SEGMENT: ANTE: Abstracts in New Technologies and Engineering

Data processor including an A / D converter **for** converting **a** plurality **of** analog **input** channels **into digital data**

ABSTRACT:
A data processor includes a CPU and an **A / D converter** for **converting** one of several analog inputs into digital data. A data memory stores data designating analog inputs to be converted. A circuit, responsive to an **A / D conversion** completion signal from the **A / D converter** , supplies a macro service operation request to the CPU, which interrupts the CPU without having...

...contents of a CPU program counter and a CPU status register. Upon completion of the **A / D conversion** , the **converted** digital data are stored in a predetermined location, and CPU execution resumes.

DESCRIPTORS: Central processing units; Digital data; Converters; Conversion ; **Analog** to **digital converters** ; Microprocessors; Interrupts; **Channels** ; Circuits; Registers

15/3,K/12 (Item 3 from file: 60)
DIALOG(R)File 60:ANTE: Abstracts in New Tech & Engineer
(c) 2009 CSA. All rts. reserv.

0001556893 IP ACCESSION NO: 20081186974
Arrangement for converting a plurality of electrical analog measurement signals that are applied simultaneously to its input terminals into a corresponding plurality of digital signals, using an antialiasing filter on the inputs

Sezi, Tevfik

, USA
PUBLISHER URL:
http://patft.uspto.gov/netacgi/nph-Parser?Sect1=PTO2&Sect2=HITOFF&u=/netahtml/PTO/search-adv.htm&r=1&p=1&f=G&l=50&d=PTXT&S1=5412386.PN.&OS=pn/5412386&RS=PN/5412386

DOCUMENT TYPE: Patent
RECORD TYPE: Abstract
LANGUAGE: English
FILE SEGMENT: ANTE: Abstracts in New Technologies and Engineering

ABSTRACT:
... which have at least two downstream sample-and-hold circuits connected to them. At least **two analog - digital converters** are **linked** on the input side to the output of a sample-and-hold circuit. An evaluation device is arranged downstream from the at least two **analog - digital converters** and acquires in one evaluation interval (0 through T1) digital values corresponding to several sampling...

DESCRIPTORS: Circuits; Multiplexers; **Analog** to **digital converters** ; Positioning; **Converters** ; Terminals; Sampling; Inventions; Electrical measurement; Analog circuits; Control equipment

15/3,K/13 (Item 4 from file: 60)
DIALOG(R)File 60:ANTE: Abstracts in New Tech & Engineer
(c) 2009 CSA. All rts. reserv.

0001552967 IP ACCESSION NO: 20081014846
Real-time computerized engine analyzer using multiple analog **-to-** digital conversion **system**

Mueller, Steve; Meyers, Scott; Lambach, Chris; Stern, Glenn; Cochenet, Joseph; Werth III, John T; Rodriguez, Carlos E; Wozniak, John N; Hintz, John; Hansen, Richard W; Trottier, Steve

, USA
PUBLISHER URL:
http://patft.uspto.gov/netacgi/nph-Parser?Sect1=PTO2&Sect2=HITOFF&u=/netahtml/PTO/search-adv.htm&r=1&p=1&f=G&l=50&d=PTXT&S1=5481193.PN.&OS=pn/5481193&RS=PN/5481193

DOCUMENT TYPE: Patent

RECORD TYPE: Abstract
LANGUAGE: English
FILE SEGMENT: ANTE: Abstracts in New Technologies and Engineering

Real-time computerized engine analyzer using multiple analog **-to-** digital conversion **system**

ABSTRACT:
... into a digital waveform which is displayed on a monitor. The waveform is converted using **two analog** -to- **digital (A / D) conversion channels** . A dedicated A/D control microprocessor is used to control the flow of the digital waveform data between the **analog** -to- **digital conversion channels** and a main computer. Waveform data transfer to the main computer is over a dedicated...

DESCRIPTORS: Waveforms; Conversion; Microprocessors; **Analog** to **digital conversion** ; Monitors; **Channels** ; Engine analyzers; Engines; High speed; Data transfer (computers); Real time; Internal combustion engines

15/3,K/14 (Item 5 from file: 60)
DIALOG(R)File 60:ANTE: Abstracts in New Tech & Engineer
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0001192154 IP ACCESSION NO: 20080838877
Method and system for facilitating transmission of analog signals to a **wireless terminal**

Pope, John

, USA
PUBLISHER URL:
http://patft.uspto.gov/netacgi/nph-Parser?Sect1=PTO2&Sect2=HITOFF&u=/netahtml/PTO/search-adv.htm&r=1&p=1&f=G&l=50&d=PTXT&S1=7373118.PN.&OS=pn/7373118&RS=PN/7373118

DOCUMENT TYPE: Patent
RECORD TYPE: Abstract
LANGUAGE: English
FILE SEGMENT: ANTE: Abstracts in New Technologies and Engineering

ABSTRACT:
... the modulation frequency, the radio link converter may responsively generate an analog signal having a **plurality** of **analog channels** that defines the bearer data in the **digital** signal. The radio **link** converter may then output the analog signal to an antenna for transmission to a wireless...

DESCRIPTORS: Channels; Converters; Radio; Modulation; Terminals; **Analog** to **digital converters** ; Antennas; Wireless communication; Networks

15/3,K/15 (Item 6 from file: 60)
DIALOG(R)File 60:ANTE: Abstracts in New Tech & Engineer
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0001117442 IP ACCESSION NO: 2008730319
Video composite transmission system integrating encoded data channels into blanking and synchronizing signal

Briand, Marcel E; Pannetier, Georges A

, USA
PUBLISHER URL:
http://patft.uspto.gov/netacgi/nph-Parser?Sect1=PTO2&Sect2=HITOFF&u=/netahtml/PTO/search-adv.htm&r=1&p=1&f=G&l=50&d=PTXT&S1=4191969.PN.&OS=pn/4191969&RS=PN/4191969

DOCUMENT TYPE: Patent
RECORD TYPE: Abstract
LANGUAGE: English
FILE SEGMENT: ANTE: Abstracts in New Technologies and Engineering

ABSTRACT:
... transmitting device and a plurality of data terminals to a video switching network via an **analog two path line** transmitting an analog video composite signal. In the transmission part, it comprises means for shortening...

...and synchronizing signal, in elongated back blanking porches of which are integrated and companded first **digital multiplex** data **channels** transmitted from first data terminals. Second **digital multiplex** data **channels** are also integrated and companded into the trace interval of each available black line of vertical blanking and synchronizing signal transmitted from camera. The first and second **digital multiplex** companded data **channels** are mixed and converted in a multilevel code, and the multilevel coded channel is analogically...

...obtain said analog video composite signal. The receiving part of the system enables each initial **digital** data **channel** and the initial blanking and synchronizing signal to be reconstituted in response to the analog...

...DESCRIPTORS: Channels; Synchronism; Cameras; Multilevel; Terminals; Video signals; Transmission; Switching; Networks; Switching theory; Elongation; Digital data; **Analog** to **digital converters** ; Receivers; Joining

15/3,K/16 (Item 7 from file: 60)
DIALOG(R)File 60:ANTE: Abstracts in New Tech & Engineer

0000878597 IP ACCESSION NO: 2008654990
Multi-channel transceiver having an adaptive antenna array and method

Smith, Paul Fielding; Harrison, Robert Mark

, USA
PUBLISHER URL:
http://patft.uspto.gov/netacgi/nph-Parser?Sect1=PTO2&Sect2=HITOFF&u=/netahtml/PTO/search-adv.htm&r=1&p=1&f=G&l=50&d=PTXT&S1=5748683.PN.&OS=pn/5748683&

RS=PN/5748683

DOCUMENT TYPE: Patent
RECORD TYPE: Abstract
LANGUAGE: English
FILE SEGMENT: ANTE: Abstracts in New Technologies and Engineering

DESCRIPTORS: Adaptive antenna **arrays** ; Radio frequencies; Transceivers; **Analog** to **digital converters** ; **Channels** ; Inventions; Communication systems; Splitting; Receivers; Transmitters; Digital to analog conversion

15/3,K/17 (Item 8 from file: 60)
DIALOG(R)File 60:ANTE: Abstracts in New Tech & Engineer
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0000483645 IP ACCESSION NO: 2008009460
Cross-path calibration for data acquisition using multiple digitizing paths

Zhuge, James

, USA
PUBLISHER URL:
http://patft.uspto.gov/netacgi/nph-Parser?Sect1=PTO2&Sect2=HITOFF&u=/netahtml/PTO/search-adv.htm&r=1&p=1&f=G&l=50&d=PTXT&S1=7302354.PN.&OS=pn/7302354&RS=PN/7302354

DOCUMENT TYPE: Patent
RECORD TYPE: Abstract
LANGUAGE: English
FILE SEGMENT: ANTE: Abstracts in New Technologies and Engineering

ABSTRACT:
The present invention utilizes **multiple** A/D (**analog** -to- **digital**) **paths** and cross- **path** calibration to provide accurate and reliable measurements for each input channel in a data acquisition...
...10 volts), while the second path includes a high-gain amplifier. Each path includes an **analog** -to- **digital converter** (**ADC**), so that there is a one-to-one correspondence between the number of paths and...

DESCRIPTORS: Calibration; Channels; **Analog** to **digital conversion** ; Inventions; Crystals; Digitizing; Amplifiers; Converters; Reduction

15/3,K/18 (Item 1 from file: 108)
DIALOG(R)File 108:Aerospace and High Technology Database
(c) 2009 CSA. All rts. reserv.

0001535159 IP ACCESSION NO: N88-28221
Multichannel data transmission through a fiber optic cable (M.S. Thesis)

HATZIDAKIS, FOKION
Naval Postgraduate School, Monterey, CA.
PUBLICATION DATE: 1987

CONFERENCE:

, UNITED STATES

RECORD TYPE: Abstract
LANGUAGE: ENGLISH
REPORT NO: AD-A193842
FILE SEGMENT: Aerospace & High Technology

ABSTRACT:
... this thesis was to design and construct a system which transmits and receives data from **different analog channels** through a single fiber optic cable link. The system uses a microprocessor controlled multiplexer and a high speed **analog** -to- **digital converter** . Tests and measurements were performed to examine the restrictions, problems and different options on the...

DESCRIPTORS: ***Analog** to **digital converters** ; * **Channels** (data transmission); *Data transmission; *Fiber optics; *Light transmission; *Microprocessors; *Multichannel communication; *Multiplexing; *Optical communication; *Transmission...

15/3,K/19 (Item 2 from file: 108)
DIALOG(R)File 108:Aerospace and High Technology Database

0000862329 IP ACCESSION NO: A78-37404
Data acquisition and control equipment for studying unsteady flow in an axial compressor

WALKER, G J
Tasmania, University, Hobart, Australia [WALKER]
PUBLICATION DATE: 1977

CONFERENCE:
Institution of Engineers, Australian Hydraulics and Fluid Mechanics Conference, 6th, Adelaide, Australia, Australia, 5-9 Dec. 1977

DOCUMENT TYPE: Conference Paper
RECORD TYPE: Abstract
LANGUAGE: English
FILE SEGMENT: Aerospace & High Technology

ABSTRACT:
... determined to within 0.1%. Data are evaluated by a computer system consisting of 16 **analog** input **channels** , with **two** 8-channel multiplexers and a 12-bit **A / D converter** with a 47 kHz sampling rate. Compressor speed was regulated by a thyristor-controlled adjustable...

DESCRIPTORS: *Control equipment; *Data acquisition; *Engine control; *Flow measurement; *Turbocompressors; *Unsteady flow; **Analog** to **digital converters** ; **Channels** (data transmission); Computer techniques; Data correlation; Data sampling; Direct current; Electric motors; Thyristors

15/3,K/20 (Item 3 from file: 108)
DIALOG(R)File 108:Aerospace and High Technology Database

0000392755 IP ACCESSION NO: A69-35745
A high-speed digital data acquisition system (High speed analog **to**
digital multiple channel **wideband data acquisition system designed for**
short pulse Doppler radar and probe measurements)

REINAGEL, F G; TRIPP, B R
CORNELL AERONATICAL LAB., INC., ELECTRONICS RESEARCH DEPT., BUFFALO, N.Y.
[REINAGEL, TRIPP]

PAGES: 4P
PUBLICATION DATE: 1969

PUBLISHER: NEW YORK: INST. OF ELECTRICAL AND ELECTRONICS ENGINEERS, INC.

CONFERENCE:
, United States

RECORD TYPE: Citation
LANGUAGE: English
FILE SEGMENT: Aerospace & High Technology
A high-speed digital data acquisition system (High speed analog **to**
digital multiple channel **wideband data acquisition system designed for**
short pulse Doppler radar and probe measurements)

DESCRIPTORS: ***Analog** to **digital converters** ; *Data acquisition;
*Digital systems; *Electrostatic probes; *Radar data; Broadband;
Conferences; Data reduction; Doppler radar; Pulse...
?

19/3,K/1 (Item 1 from file: 99)
DIALOG(R)File 99:Wilson Appl. Sci & Tech Abs
(c) 2009 The HW Wilson Co. All rts. reserv.

1283877 H.W. WILSON RECORD NUMBER: BAST96006050
VME boards provide conversion for digital receivers
AUGMENTED TITLE: 6400 series of **A / D converters** from Pentek Inc.
Schweber, Bill;
EDN v. 40 (Dec. 21 '95) p. 18
DOCUMENT TYPE: Product Evaluation ISSN: 0012-7515

AUGMENTED TITLE: 6400 series of **A / D converters** from Pentek Inc.

ABSTRACT: The 6400 series of **analog** -to- **digital converter** boards from Pentek Inc., Norwood, New Jersey, is described. The converters feature single-slot 6U boards, which differ from each other mainly in resolution and sampling rate. Each includes 2 **matched analog** -to- **digital channels** , input-signal conditioning, antialiasing lowpass filters, and clock-generation circuitry. The common clock results in...

DESCRIPTORS: **Analog - digital converters** ; ;

^ 19/3,K/2 (Item 1 from file: 60)
DIALOG(R)File 60:ANTE: Abstracts in New Tech & Engineer
(c) 2009 CSA. All rts. reserv.

0001680958 IP ACCESSION NO: 20081380665
Circuit and process for chrominance decoding with analog **or** digital **delay** line **in a television system of a pal or secam type**

Douziech, Patrick; Imbert, Michel

, USA
PUBLISHER URL:
http://patft.uspto.gov/netacgi/nph-Parser?Sect1=PTO2&Sect2=HITOFF&u=/netahtml/PTO/search-adv.htm&r=1&p=1&f=G&l=50&d=PTXT&S1=4553156.PN.&OS=pn/4553156&RS=PN/4553156

DOCUMENT TYPE: Patent
RECORD TYPE: Abstract
LANGUAGE: English
FILE SEGMENT: ANTE: Abstracts in New Technologies and Engineering

Circuit and process for chrominance decoding with analog **or** digital **delay** line **in a television system of a pal or secam type**

ABSTRACT:
... circuit for connecting a chrominance decoding integrated circuit normally connected by terminals to a conventional **analog** delay **line** so as to make it compatible with a **digital** delay **line** . This **matching** circuit comprises a switch connecting alternately each of the outputs of the integrated circuit to an **analog - digital convertor** connected to a **digital** delay **line** , to a digital-analog convertor, then to a switch routing the signal alternately to each...

20/3,K/1 (Item 1 from file: 60)
DIALOG(R)File 60:ANTE: Abstracts in New Tech & Engineer
(c) 2009 CSA. All rts. reserv.

0001816554 IP ACCESSION NO: 20081687160
Communication system analog **-to-** digital converter **using echo information to improve resolution**

Agazzi, Oscar E

, USA
PUBLISHER URL:
http://patft.uspto.gov/netacgi/nph-Parser?Sect1=PTO2&Sect2=HITOFF&u=/netahtml/PTO/search-adv.htm&r=1&p=1&f=G&l=50&d=PTXT&S1=4999830.PN.&OS=pn/4999830&RS=PN/4999830

DOCUMENT TYPE: Patent
RECORD TYPE: Abstract
LANGUAGE: English
FILE SEGMENT: ANTE: Abstracts in New Technologies and Engineering

Communication system analog **-to-** digital converter **using echo information to improve resolution**

Agazzi, Oscar E

ABSTRACT:
... has at least one terminal that simultaneously applies an analog signal corresponding to a first **digital** stream to the **link** and converts an **analog** signal from the **link** into a second digital stream. The analog signal received from the link has a near...

DESCRIPTORS: **Analog** to **digital converters** ; Streams; Communication systems; Terminals; Exchanging; **Analog** to **digital conversion** ; Forming; Bells; Converters

20/3,K/2 (Item 1 from file: 108)
DIALOG(R)File 108:Aerospace and High Technology Database
(c) 2009 CSA. All rts. reserv.

0004210229 IP ACCESSION NO: A08-99-1790829
Communication system analog **-to-** digital converter **using echo information to improve resolution**

Agazzi, Oscar E

, USA
PUBLISHER URL:
http://patft.uspto.gov/netacgi/nph-Parser?Sect1=PTO2&Sect2=HITOFF&u=/netahtml/PTO/search-adv.htm&r=1&p=1&f=G&l=50&d=PTXT&S1=4999830.PN.&OS=pn/4999830&RS=PN/4999830

DOCUMENT TYPE: Patent
RECORD TYPE: Abstract

LANGUAGE: English
FILE SEGMENT: Aerospace & High Technology

Communication system analog **-to-** digital converter **using echo information to improve resolution**

Agazzi, Oscar E

ABSTRACT:
... has at least one terminal that simultaneously applies an analog signal corresponding to a first **digital** stream to the **link** and converts an **analog** signal from the **link** into a second digital stream. The analog signal received from the link has a near...

DESCRIPTORS: **Analog** to **digital converters** ; Streams; Communication systems; Terminals; Exchanging; **Analog** to **digital conversion** ; Forming; Bells; Converters

Patent Files:-

File 344:Chinese Patents Abs Jan 1985-2006/Jan
(c) 2006 European Patent Office
File 347:JAPIO Dec 1976-2008/Oct(Updated 090220)
(c) 2009 JPO & JAPIO
File 350:Derwent WPIX 1963-2008/UD=200913
(c) 2009 Thomson Reuters

Set	Items	Description
S1	13121	DIGITAL(3W)(CHANNEL??? OR PATH??? OR LINK??? OR LINES)
S2	3875	ANALOG(3W)(PATH??? OR LINK??? OR LINES OR CHANNEL??? OR CHANEL???)
S3	139775	ADC OR (ANALOG(2W)DIGITAL OR A()D)(2W)CONVER??????
S4	2891	(PLURAL? OR MANY OR MULTI OR MULTIPLE? ? OR NUMEROUS?? OR SEVERAL? ? OR DIFFERENT?? OR TWO OR ARRAY??)(3N)(S1 OR S2)
S5	175	(SMALLER OR LOWER OR LESS???)(9N)(S1 OR S2)
S6	156	(GREATER OR HIGHER OR LARGER OR BIGGER)(9N)(S1 OR S2)
S7	110	AU=(AGAZZI O? OR AGAZZI, O? OR GOPINATHAN V? OR GAPINATHAN, V?)
S8	168	(MATCH??? OR COMPAR???)(5N)(S1 OR S2)
S9	4	S1 AND S2 AND S3 AND S4 AND (S5 OR S6)
S10	20	S1 AND S2 AND S3 AND (S5 OR S6)
S11	16	S10 NOT S9
S12	10	S1 AND S2 AND S3 AND S8
S13	9	S12 NOT (S9 OR S10)
S14	2	S7 AND S1 AND S2 AND S3

9/3,K/1 (Item 1 from file: 350)
DIALOG(R)File 350:Derwent WPIX

0011066024 - Drawing available
WPI ACC NO: 2002-001034/200201
Related WPI Acc No: 2001-089171; 2001-520956; 2002-172879; 2002-255311; 2002-405668; 2005-402141
XRPX Acc No: N2002-000758
Antenna system for tower-top installation, comprises corporate feed for operatively interconnecting antenna elements with backhaul link
Patent Assignee: ANDREW AG (ANDC); ANDREW CORP (ANDC)
Inventor: JACKSON D G; JUDD M D; MACA G A
Patent Family (8 patents, 29 countries)

Patent Number	Kind	Application Date	Number	Kind	Date	Update
EP 1143554	A2	20011010	EP 2001105409	A	20010312	200201 B
CA 2340146	A1	20010930	CA 2340146	A	20010309	200201 E
JP 2001332928	A	20011130	JP 200195482	A	20010329	200202 E
US 6701137	B1	20040302	US 1999299850	A	19990426	200417 E
			US 1999422418	A	19991021	
			US 2000538955	A	20000331	
EP 1143554	B1	20051228	EP 2001105409	A	20010312	200605 E
DE 60116174	E	20060202	DE 60116174	A	20010312	200615 E
			EP 2001105409	A	20010312	
DE 60116174	T2	20060831	DE 60116174	A	20010312	200660 E
			EP 2001105409	A	20010312	
CA 2340146	C	20061010	CA 2340146	A	20010309	200668 E

Priority Applications (no., kind, date): US 1999299850 A 19990426; US 1999422418 A 19991021; US 2000538955 A 20000331; EP 2001105409 A 20010312

Original Publication Data by Authority

Argentina

Assignee name & address:
Claims:
...including a high speed multiplexer for de-multiplexing a high speed digital signal into M **lower** speed **digital** signals to be fed to the M columns of antenna elements; **analog / digital conversion** circuitry (**28** ;228,264) for converting between analog and digital representations of the backhaul signals;frequency conversion...

...signals and intermediate frequency signals;the radio frequency circuits configured for providing the necessary processing **of radio frequency** communication signals between said antenna **array** and **said** backhaul **link** for transceiving communication signals with said ground-based equipment in one of the digital baseband a...including:multiplexing circuitry for multiplexing between the backhaul link and multiple antenna elements of the **array** ; **analog / digital** conversion circuitry for converting between analog **and** digital representations **of** the backhaul signals;frequency conversion circuitry for converting between radio frequency communication signals and intermediate...

...for transceiving communication signals with said ground-based equipment in one of the digital baseband **and** digital IF **formats** on the backhaul link.

9/3,K/2 (Item 2 from file: 350)
DIALOG(R)File 350:Derwent WPIX

0010274147 - Drawing available
WPI ACC NO: 2000-587003/200055
XRPX Acc No: N2000-434462
Signal generator for digital hearing aid, has delay device in any one of microphone channels to output delayed bit stream signals, whose operation is regulated by signal processor
Patent Assignee: TOEPHOLM & WESTERMANN APS (TOEP-N); WIDEX AS (WIDE-N)
Inventor: ANDERSEN H H; LUDVIGSEN C
Patent Family (9 patents, 22 countries)

Patent Number	Kind	Date	Application Number	Kind	Date	Update
WO 2000047015	A1	20000810	WO 1999EP767	A	19990205	200055 B
AU 199928317	A	20000825	AU 199928317	A	19990205	200059 E
			WO 1999EP767	A	19990205	
EP 1097607	A1	20010509	EP 1999908852	A	19990205	200128 E
			WO 1999EP767	A	19990205	
US 6339647	B1	20020115	WO 1999EP767	A	19990205	200208 E
			US 2001763692	A	20010226	
JP 2002536931	W	20021029	WO 1999EP767	A	19990205	200274 E
			JP 2000597977	A	19990205	
AU 753295	B	20021017	AU 199928317	A	19990205	200280 E
			WO 1999EP767	A	19990205	
EP 1097607	B1	20030416	EP 1999908852	A	19990205	200328 E
			WO 1999EP767	A	19990205	
DE 69906979	E	20030522	DE 69906979	A	19990205	200341 E
			EP 1999908852	A	19990205	
			WO 1999EP767	A	19990205	
CA 2341255	C	20030909	CA 2341255	A	19990205	200361 E
			WO 1999EP767	A	19990205	

Priority Applications (no., kind, date): WO 1999EP767 A 19990205

Alerting Abstract ...1a,1b) for microphones (2a,2b), have primary or secondary or higher order sigma-delta **analog - digital converters** (3a,3b). The single bit high clock frequency is converted into a digital word sequence...
...3a,3b Sigma-delta **analog - digital converters**

Original Publication Data by Authority

Argentina

Assignee name & address:
Original Abstracts:
...1a, 1b) for at least two microphones (2a, 2b), said microphone channels

comprising each an **analog** to **digital converter** (**3a** , 3b) **and having** at least one programmable or program controlled signal processor (5), as well as a digital to **analog converter** , **and** at least **one** receiver and a battery for power supply. The invention particularly comprises in each microphone channel (1a, 1b) a sigma-delta-type **analog** to **digital converter** (**3a** , 3b) **including a** digital low pass filter and a decimator (4) for converting a 1 Bit Stream of...

...one signal processor (5). Preferably the delay device (6) is integrated into said sigma-delta- **ADC** (3).

...
...1a, 1b) for at least two microphones (2a, 2b), the microphone channels each comprising an **analog** to **digital converter** (3a, 3b) and having at least one programmable or program controlled signal processor (5), as well as a digital to **analog converter** , and **at least** one receiver and a battery for power supply. The hearing aid particularly comprises in each microphone channel (1a, 1b) a sigma-delta-type **analog** to **digital converter** (3a, 3b) including a digital low pas filter and a decimator 94) for converting a 1 Bit Stream of a high clock frequency into a **digital word** sequence of a **lower** clock frequency. At least one of the at least two microphone channels **contains** a **controllable delay** device (6) connected to the input side of the respective digital low pass filter and...

...least one signal processor (5). The delay device is preferably integrated into the sigma-delta- **ADC** (3...

...The invention relates to a hearing aid with beam forming properties, having at least two **microphone** channels (1a, 1b) for at least two microphones (2a, 2b), said microphone channels comprising each an **analog** to **digital converter** (3a, 3b) and having at least one programmable or program controlled signal processor (5), as...
...supply. The invention particularly comprises in each microphone channel (1a, 1b) a sigma-delta-type **analog** to **digital converter** (**3a** , 3b) **including** a digital low pass filter and a decimator (4) for converting a 1 Bit Stream **of** a **high clock** frequency into a digital word sequence of a **lower** clock frequency.At least one of said at least **two** microphone **channels** contains a controllable delay device (6) connected to the input side of the respective digital low pass filter and decimator (4) of said channel, said delay **device** (6) **being controllable** by said at least one signal processor (5). Preferably the delay device (6) is integrated into said sigma-delta- **ADC** (3...

...prothese auditive dotee de proprietes de formation de faisceaux, qui possede au moins deux voies **micro** (1a, 1b) destinees a au moins deux microphones (2a, 2b), lesdites voies micro comportant chacune
Claims:
...mocrophone channels (1a, 1b) for at least two microphones (2a, 2b/, said microphone channels comprising **each** an **analog** to **digital converter** (**3a** , 3b) and having **at** least **one programmable** or program controlled digital signal processor (6), as well as a digital to analog converter...

...power supply, characterized in that each microphone channel (1a, 1b) contains a sigma-delta-type **analog** to **digital converter** (3a, 3b)

including a digital low **pass** filter **and decimator** (4) for converting a 1 Bit stream of a high clock frequency into a digital...

...battery for power supply, wherein each microphone channel (1a, 1b) contains a sigma-delta-type **analog** to **digital converter** (3a, 3b), a digital low pass filter and decimator (4) for converting a 1 Bit...

...and at least one of said at least two microphone channels contains a controllable delay **device** (6) **connected to** the input side of the respective digital low pass filter and decimator (4) **of** said **channel** , said delay device (6) being controllable by said processor (5).

9/3,K/3 (Item 3 from file: 350)
DIALOG(R)File 350:Derwent WPIX
(c) 2009 Thomson Reuters. All rts. reserv.

0008987280 - Drawing available
WPI ACC NO: 1998-541958/199846
XRPX Acc No: N1998-421883
Flash type analog **current to** digital **voltage** converter **- performs feedback switching of selected reference current multiple to parallel channels when digital output bit of particular channel is at higher significant level**
Patent Assignee: INT BUSINESS MACHINES CORP (IBMC)
Inventor: FRANKENY R F; SMADI M M
Patent Family (1 patents, 1 countries)

Patent Number	Kind	Application Date	Number	Kind	Date	Update
US 5815107	A	19980929	US 1996770603	A	19961219	199846 B

Priority Applications (no., kind, date): US 1996770603 A 19961219

Patent Details

Number	Kind	Lan	Pg	Dwg	Filing Notes
US 5815107	A	EN	11	7	

Flash type analog **current to** digital **voltage** converter **-**

Alerting Abstract ...ADVANTAGE - Performs highly accurate **analog** current to **digital** voltage **conversion** within one switch period. Facilitates direct analog current to digital binary coded decimal conversion through...

Original Publication Data by Authority

Argentina

Assignee name & address:
Original Abstracts:
An architecture for a high speed **analog** current to **digital voltage converter** particularly **suited** for **integrated** circuit applications. As preferably implemented, an analog signal of current form and an associated reference...

...are generated on a source integrated chip. The reference current line and one or more **analog** current **lines** transmit **data** between **the** source and a receiving integrated circuit chips. The high speed converter utilizes current mirrors to...

...bits. Since switching of lower order bits by higher order bits is accomplished simultaneously, the **analog** current to **digital voltage conversion** is **accomplished** within **one** switch period while retaining the relatively high accuracy.
Claims:
Analog to **digital converter responsive to** an input current, comprising: means for generating an input signal proportioned to the analog input...

...two or more parallel channels to concurrently compare in each of the parallel channels the **analog** input current with **multiples** of a reference current, the parallel channels being individually associated with **digital output** bits of the integrated circuit chip; and means for feedback switching, during the concurrent compare selected ones of the reference current multiples in a parallel channel responsive to a **state** of a **digital output** bit at a **higher** level of significance.

9/3,K/4 (Item 4 from file: 350)

0008038039 - Drawing available
WPI ACC NO: 1997-131936/199712
XRPX Acc No: N1997-108962
Magnetic resonance imaging system having read gradient scaler for scaling amplitude and width of read gradients - has device for controlling sampling rate of resonance signals received from corresp. magnetic resonance echoes, and thus changes bandwidth of data acquisition rates from echo to echo in common range
Patent Assignee: MARCONI MEDICAL SYSTEMS INC (MAON); PICKER INT INC (PXRM)
Inventor: GULLAPALLI R P; LIU H; LONCAR M J
Patent Family (6 patents, 3 countries)

Patent Number	Kind	Date	Application Number	Kind	Date	Update
US 5602476	A	19970211	US 1995516386	A	19950817	199712 B
EP 759562	A2	19970226	EP 1996305556	A	19960729	199714 E
JP 9056696	A	19970304	JP 1996231457	A	19960813	199719 E
EP 759562	A3	19970416	EP 1996305556	A	19960729	199729 E
EP 759562	B1	20021016	EP 1996305556	A	19960729	200276 E
DE 69624303	E	20021121	DE 69624303	A	19960729	200302 E
			EP 1996305556	A	19960729	

Priority Applications (no., kind, date): US 1995516386 A 19950817

Alerting Abstract ...magnetic resonance signals to produce a series of data lines, and is associated with an **analog** -to- **digital converter** such that the data lines are digital. A data memory stores the **digital**

data **lines** , and a reconstruction processor reconstructs the data lines from the data memory into an image...

...and negative phase-encoding angles have the highest bandwidth. A data line sorter sorts the **digital** data **lines** in accordance with bandwidth and supplies the sorted data lines to the data memory...

Original Publication Data by Authority

Argentina

Assignee name & address:
Claims:
...presence of a read gradient, the magnetic resonance echoes are digitized and demodulated to form **digital** data **lines** , the **data lines** are stored and reconstructed by a reconstruction algorithm to generate an image representation, characterized by...

...to generate a second digital data line of a second bandwidth different from the first **bandwidth** , the **digital** data **lines** of **the** first **and** second bandwidths being reconstructed to form a common resultant image representation...

...presence of a read gradient, the magnetic resonance echoes are digitized and demodulated to form **digital** data **lines** , the data lines are stored and reconstructed by a reconstruction algorithm **to** generate **an** image representation, which includes the steps of reading-out a first of the magnetic resonance...
...a second digital data line of a second bandwidth different from the first bandwidth, the **digital data lines** of the first and second bandwidths being reconstructed into one resultant **image** representation, **characterised** in that the data line with **lower** bandwidth is phase-encoded with a smaller phase-encoding angle and the data line with... resonance signals to produce a series of data lines, the receiver being associated with an **analog** -to- **digital converter** such that the data lines are digital, a data memory which stores the **digital** data **lines** , and a reconstruction processor which reconstructs **the** data **lines from** the data memory into an image representation, the improvement comprising:a read gradient **scaler** which **scales** amplitude and width of selected read gradient pulses such that a bandwidth of the radio...
?

^11/3,K/1 (Item 1 from file: 347)
DIALOG(R)File 347:JAPIO
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03730394 **Image available**
DIGITAL ELECTRONIC KEY TELEPHONE SYSTEM

PUB. NO.: 04-095494 [JP 4095494 A]
PUBLISHED: March 27, 1992 (19920327)
INVENTOR(s): SANHONGI TOSHIRO
SASAGUCHI ATSUMI
APPLICANT(s): MATSUSHITA ELECTRIC IND CO LTD [000582] (A Japanese Company or Corporation), JP (Japan)
APPL. NO.: 02-212881 [JP 90212881]
FILED: August 10, 1990 (19900810)
JOURNAL: Section: E, Section No. 1234, Vol. 16, No. 324, Pg. 105, July 15, 1992 (19920715)

ABSTRACT

... general analog individual telephone sets 4a-4m not through an adapter. Further, the number of **analog / digital converting** means 6a and 6b is **less** than the number of **analog channels** and **digital channels** , so one means 6a and one means 6b are not necessary for the **analog channels** and the digital electronic key telephone system 100 can be constituted at low cost.

11/3,K/2 (Item 1 from file: 350)
DIALOG(R)File 350:Derwent WPIX
(c) 2009 Thomson Reuters. All rts. reserv.

0015444570 - Drawing available
WPI ACC NO: 2005-794246/200581
XRAM Acc No: C2005-244869
XRPX Acc No: N2005-657891
Circuitry for monitoring electrochemical process e.g. copper deposition process, in electrochemical cell, comprises microcontroller for switching between galvanostatic and potentiostatic modes of operation of electrochemical cell
Patent Assignee: ADVANCED TECHNOLOGY MATERIALS (ADTE-N); LURCOTT S (LURC-I); TOM G M (TOMG-I)
Inventor: LURCOTT S; TOM G M; TOM G
Patent Family (5 patents, 109 countries)

Patent	Application				
Number	Kind	Date	Number	Kind	Date	Update
US 20050247576	A1	20051110	US 2004838390	A	20040504	200581 B
WO 2005111592	A2	20051124	WO 2005US13772	A	20050422	200581 E
EP 1749204	A2	20070207	EP 2005738835	A	20050422	200713 E
			WO 2005US13772	A	20050422	
KR 2007017548	A	20070212	KR 2006725544	A	20061204	200755 E
			WO 2005US13772	A	20050422	
US 7427346	B2	20080923	US 2004838390	A	20040504	200863 E

Priority Applications (no., kind, date): US 2004838390 A 20040504

Alerting Abstract ...ADC1, ADC2 **Analog** -to- **digital converter**

Technology Focus

...circuitry is within a potential range of the unipolar power supply. It further comprises two **analog** -to- **digital converters** (ADC1, ADC2), two digital-to-analog converters (DAC, DAC2), operational amplifier (OpAmp), and current measurement scaling unit. The first **analog** -to- **digital converter** is arranged to input to the microcontroller (uController) a first digital signal correlative of voltage in the electrochemical cell. The second **analog** -to- **digital converter** is arranged to input to the microcontroller a first digital signal correlative of current passing through the electrochemical cell. The first **digital** -to- **analog** converter **linked** to the microcontroller for receiving a potential control digital signal from the microcontroller, and to...

...current in the potentiostatic mode of operation of the electrochemical cell. The second digital-to- **analog** converter is **linked** to the microcontroller for receiving an offset voltage digital signal from the microcontroller and responsively...

...potentiostatic measurement of response of the electrochemical cell, and an output linked to the second **analog** -to **digital converter** for transmission of an output signal to the second **analog** -to- **digital converter** . The operational amplifier is arranged to amplify current required to maintain the offset voltage in...

...circuitry. The circuitry further comprises a buffer linked between the electrochemical cell and the first **analog** -to- **digital converter** .

Original Publication Data by Authority

Argentina

Assignee name & address:
Claims:
...connectable to one another for said potentiostatic mode of operation, a current control digital-to- **analog** converter arranged for **linking** to said working electrode and to said CMOS analog switch, and adapted to bring the...

...predetermined current condition for said galvanostatic mode of operation, and a potential control digital-to- **analog** converter arranged for **linking** to said CMOS analog switch and to said reference electrode, and adapted to bring the...

...of operation, and to said predetermined potential condition in said potentiostatic mode of operation, of **less** than one millisecond, and with said CMOS **analog** switch arranged for **linking** with said counter electrode.

11/3,K/3 (Item 2 from file: 350)

0013505260 - Drawing available

WPI ACC NO: 2003-597834/200356
XRPX Acc No: N2003-476499
Power consumption reducing method for digital subscriber line drivers, involves producing analog waveform from bi-level sequence that is created by delta-sigma modulator from an oversampled signal
Patent Assignee: GLOBESPAN VIRATA INC (GLOB-N); KEASLER W E (KEAS-I)
Inventor: KEASLER W E
Patent Family (2 patents, 1 countries)
Patent Application
Number Kind Date Number Kind Date Update
US 20030128144 A1 20030710 US 2002345832 P 20020104 200356 B
US 2003336922 A 20030106
US 6741196 B2 20040525 US 2003336922 A 20030106 200435 E

Priority Applications (no., kind, date): US 2002345832 P 20020104; US 2003336922 A 20030106

Patent Details
Number Kind Lan Pg Dwg Filing Notes
US 20030128144 A1 EN 9 5 Related to Provisional US 2002345832
Original Publication Data by Authority

Argentina

Assignee name & address:
Original Abstracts:
...comprise a multi stage delta-sigma modulator with a high current 1-bit digital-to- **analog converter** (**DAC**) output stage. **By** adding the high current drive capability to the 1-bit DAC in a delta-sigma digital-to- **analog converter the** traditional DSL **line** driver used in **digital** subscriber **lines** applications **is** made **less** complex and it **saves** on the overall power consumption. The invention uses a transistor switch arrangement to save the...

...bit DAC in a delta-sigma digital-to-analog converter the traditional DSL line driver **used** in **digital subscriber lines** applications is made **less** complex and **it** saves **on** the overall power **consumption** . The invention uses a transistor switch arrangement to save the overall power by alternately switching...
Claims:

11/3,K/4 (Item 3 from file: 350)
DIALOG(R)File 350:Derwent WPIX
(c) 2009 Thomson Reuters. All rts. reserv.

0013493086 - Drawing available
WPI ACC NO: 2003-585410/200355
XRPX Acc No: N2003-466030
Sampling rate increasing method for magnetic resonance data acquisition applications, involves combining magnetic resonance data with ensemble function and separating to digitize data
Patent Assignee: COLLICK B D (COLL-I); FRIGO F J (FRIG-I); FRIGO L M (FRIG-I); GE MEDICAL SYSTEMS GLOBAL TECHNOLOGY CO (GENE); HARTLEY M R (HART-I); PETTERSSON B (PETT-I)
Inventor: COLLICK B D; FRIGO F J; FRIGO L M; HARTLEY M R; PETTERSSON B

Patent Family (2 patents, 1 countries)
Patent Application
Number Kind Date Number Kind Date Update
US 20030083568 A1 20030501 US 2001682913 A 20011031 200355 B
US 6564081 B1 20030513 US 2001682913 A 20011031 200355 E

Priority Applications (no., kind, date): US 2001682913 A 20011031

Patent Details
Number Kind Lan Pg Dwg Filing Notes
US 20030083568 A1 EN 12 7
Alerting Abstract ...ADVANTAGE - The method creates a single **digital channel** with increased bandwidth and **improves the** sampling rate for MR data acquisition...

Original Publication Data by Authority

Argentina

Assignee name & address:
Original Abstracts:
...be separated into a number of channels which can be sampled at lower rates by **analog** -to- **digital converters** . **The** output **from the converters** may then be reconstructed using one of a number of interpolation techniques to create a single **digital channel** with increased **bandwidth** . **The** single **channel** with increased bandwidth may then be used to acquire MR data with an improved sampling...

...MR signal may be separated into a number of channels which can be sampled at **lower** rates by **analog** -to- **digital converters** . The output **from** the converters **may** then **be reconstructed** using one of a number of interpolation techniques to create a single **digital channel** with increased bandwidth. The single channel with **increased bandwidth** may then be used to acquire MR data with an improved sampling rate.
Claims:

11/3,K/5 (Item 4 from file: 350)
DIALOG(R)File 350:Derwent WPIX

0012447899 - Drawing available
WPI ACC NO: 2002-393512/200242
XRPX Acc No: N2002-308563
Method and device for analog **-** digital conversion **by use of preliminary variable-gain amplification, for use in radio-frequency receivers of radio-communication systems**
Patent Assignee: FORCE P (FORC-I); MATRA NORTEL COMMUNICATIONS (NELE); MATRA NORTEL COMMUNICATIONS SAS (NELE); NORTEL NETWORKS FRANCE (NELE); VAN SCHENDEL L (VSCH-I)
Inventor: FORCE P; VAN SCHENDEL L
Patent Family (5 patents, 94 countries)
Patent Application
Number Kind Date Number Kind Date Update
WO 2002007320 A1 20020124 WO 2001FR2290 A 20010713 200242 B
AU 200177592 A 20020130 AU 200177592 A 20010713 200242 E

FR 2811831 A1 20020118 FR 20009315 A 20000717 200242 E
US 20040012513 A1 20040122 WO 2001FR2290 A 20010713 200407 E
US 2003333032 A 20030808
US 6940442 B2 20050906 WO 2001FR2290 A 20010713 200560 E
US 2003333032 A 20030808
Priority Applications (no., kind, date): FR 20009315 A 20000717

Method and device for analog **-** digital conversion **by use of preliminary variable-gain amplification, for use in radio-frequency receivers of radio ...**

Original Titles:
Analog -to- **digital conversion** method and device...

... **Analog** -to- **digital conversion** of a radiocommunication signal...

... **ANALOG** -TO- **DIGITAL CONVERSION** METHOD AND DEVICE

Alerting Abstract ...NOVELTY - The method for **analog - digital conversion** of radio-communication signal is implemented by use of an **analog - digital converter** (16) preceded by a variable-gain amplifier (15), where the frequency band of signal is...

...15) so that the power of the frequency band is below the saturation limit of **analog - digital converter** (16), and the power in the useful channel which is substantially equal to the average...
...is determined as a function of power values obtained in the absence of saturation of **analog - digital converter** . The method includes a comparison of power values to the determined average value, and a...

...of first delay after implementing a modification of a parameter of analog part upstream of **analog - digital converter** , or after a lapse of second delay after a modification of the gain of amplifier...

...USE - In methods and devices for **analog - digital conversion** of radio-communication signals, for use in radio-frequency receivers of equipment, stationary and mobile...

...16 **Analog - digital converter**

Original Publication Data by Authority

Argentina

Assignee name & address:
Original Abstracts:
A method for **analog / digital conversion** of **a radiocommunication signal** using an **analog analog / digital converter preceded by variable gain** amplifier, wherein the frequency band of the converted signal contains at least one useful channel...

...the power in the frequency band of the converted signal is less than a limit **saturation** value of the **analog / digital converter** . However, **the power in** the useful **channel** is substantially equal to a mean power level having a first predetermined value in the...

...A method for **analog / digital conversion** of a radiocommunication signal using an **analog** **analog / digital converter** preceded by variable gain amplifier, **wherein the frequency band** of the converted signal contains at least one useful channel, comprises steps for controlling the...

...frequency band of the converted signal is less than a limit saturation value of the **analog / digital converter** . However, the power in the useful **channel is substantially** equal to a mean power level having a first predetermined value in the case of...

...The invention concerns a method and a device for **analog** -to- **digital conversion** of a radiocommunication signal (S) using an **analog** -to-**digital converter** (16) **preceded by** a variable gain amplifier (15), the converted **signal** frequency **band containing** at least a useful channel, which consists in controlling the amplifier (15) gain value so...

...in the converted signal frequency band is less than a threshold saturation value of the **analog - to - digital converter** and the power in the useful channel is substantially equal **to** the **average power** level having a first predetermined value in case of static propagation in the useful channel...
Claims:
1. A method of **analog / digital conversion** of **a radiocommunication signal** with the aid of an **analog / digital converter** (16) **preceded by a** variable-gain amplifier (15), the frequency band of the converted signal containing at least one...

...band of the converted signal is less than a limit saturation value (Psat) of the **analog / digital converter** (16) and that the power in the **useful channel is** substantially equal to a desired mean power level (PCo) in the useful channel having a...

...1. A method of **analog / digital conversion** of a radiocommunication signal whose frequency band contains at least one useful channel, using an **analog / digital converter preceded by** a variable-gain amplifier which receives said signal and which has a gain of a **given value** , **the** method comprising steps for controlling the value of the gain of the amplifier in such...

...the frequency band of the signal is less than a limit saturation value of the **analog / digital converter** and that power in the useful channel is substantially **equal** to a desired mean power level in **the useful channel** having a first predetermined value in the case of static propagation in the useful channel...

11/3,K/6 (Item 5 from file: 350)

0011125237 - Drawing available
WPI ACC NO: 2002-061577/200208
XRPX Acc No: N2002-045693

Driving circuit for liquid crystal display, has total number of digital to analog converters and buffer circuits that is less than number of respective

Patent Assignee: NEC CORP (NIDE); NIPPON ELECTRIC CO (NIDE)
Inventor: IKEDA N
Patent Family (5 patents, 3 countries)

Patent Number	Kind	Date	Application Number	Kind	Date	Update
US 20010043187	A1	20011122	US 2001861650	A	20010522	200208 B
JP 2001331152	A	20011130	JP 2000149243	A	20000522	200211 E
KR 2002003276	A	20020112	KR 200127979	A	20010522	200247 E
KR 430451	B	20040510	KR 200127979	A	20010522	200458 E
US 6795051	B2	20040921	US 2001861650	A	20010522	200462 E

Priority Applications (no., kind, date): JP 2000149243 A 20000522; US 2001861650 A 20010522

Original Publication Data by Authority

Argentina

Assignee name & address:
Original Abstracts:
...for storing image data, a DAC for converting digital data from the frame memory into **analog signal** , **a** buffer circuit for performing current amplification on the output of the DAC and supplying the...
Claims:
...said frame memory into analog signal; a buffer circuit which performs current amplification on output **of** said **digital** -analog **converter** ; and a controller which controls said frame memory, said **digital - analog converter** , and outward circuits, in reply to a logic signal from outward, in which the total...

...into analog signal; a buffer circuit which performs current amplification on output of said digital- **analog converter** ; **and** a controller which controls said frame memory, said digital-analog converter, and outward circuits, in...

...buffer circuits within the driving circuit for use in driving the liquid crystal display is **less** than the number of the respective data **bus lines** , wherein the image data stored in said frame memory is supplied to said digital-analog...

...further comprising a shift register for driving the data bus lines, and a plurality of **analog switches** respectively **connected** to the data bus lines, wherein the total number of said digital-analog converters is...

11/3,K/7 (Item 6 from file: 350)
DIALOG(R)File 350:Derwent WPIX

0010901693 - Drawing available
WPI ACC NO: 2001-522508/200157
XRPX Acc No: N2001-387219

Converting analogue signal to digital signal involves combining partial analogue signals distorted in opposite manner in first and second signal paths

Patent Assignee: NEUMANN GMBH GEORG (NEUM-N)
Inventor: KERN O
Patent Family (7 patents, 20 countries)

Patent Number	Kind	Date	Application Number	Kind	Date	Update
WO 2001059932	A1	20010816	WO 2000EP1133	A	20000211	200157 B
EP 1254518	A1	20021106	EP 2000909155	A	20000211	200281 E
			WO 2000EP1133	A	20000211	
JP 2003526973	W	20030909	WO 2000EP1133	A	20000211	200360 E
			JP 2001559145	A	20000211	
US 6707402	B1	20040316	WO 2000EP1133	A	20000211	200420 E
			US 2002203162	A	20020806	
EP 1254518	B1	20040616	EP 2000909155	A	20000211	200439 E
			WO 2000EP1133	A	20000211	
DE 50006858	G	20040722	DE 50006858	A	20000211	200450 E
			EP 2000909155	A	20000211	
			WO 2000EP1133	A	20000211	
JP 3641612	B2	20050427	WO 2000EP1133	A	20000211	200529 E
			JP 2001559145	A	20000211	

Priority Applications (no., kind, date): WO 2000EP1133 A 20000211

Original Publication Data by Authority

Argentina

Assignee name & address:
Original Abstracts:
...is amplified in a first signal path (2, 3, 5) and is subject to an **analog** -to- **digital conversion** (**5**). An additional **analogous** signal (S4) is obtained in a second signal path (4, 6) for transmitting greater signal amplitudes. Said signal (S4) is subject to an **analog** -to- **digital conversion** (**6**). The **signal** (**S5**) that is digitised in the first signal path (2, 3, 5) and the signal (S6...

...S1) to a digital output signal (S7), the analog input signal (S1) is amplified in **a** first signal **path** (2, 3, 5) and is subjected to an **analog** -to- **digital conversion** (5). In a second signal path (4, 6), another analog signal (S4) is obtained for transmitting **larger** signal **amplitudes and** is subjected to an **analog** -to- **digital conversion** (6). The signal (S5) digitized **in** the first signal **path** (2, 3, 5) and the **signal** (S6) that is digitized in the second **signal path** (**4** , **6**) are fed to a digital signal processor (7), which generates the **digital** output signal (**S7**). To avoid an abrupt reduction in the signal resolution and achieve the highest possible dynamic scope, it is suggested that the analog signal fed to the second signal **path** (4, 5) be distorted non-linear and counter to the amplified analog signal (S2) in...

...5). In this way, the differential amplification of the first signal path and the second **signal path** increases above a predetermined threshold and with rising signal amplitude. As a result, a non...

...is amplified in a first signal path (2, 3, 5) and is subject to an **analog** -to- **digital conversion** (5). An additional analogous signal (S4) is obtained in a second signal path (4, 6) for transmitting greater signal amplitudes. Said signal (S4) is subject to an **analog** -to- **digital conversion** (6). The signal (S5) that is digitised **in** the first signal **path** (2, 3, 5) and the signal (S6) that is digitised in the second signal path (4, 6) are supplied **to** a **digit**al signal processor (7) which generates the digital output signal (S7). The aim of the invention is to prevent abrupt reduction of the signal resolution and to obtain a **dynamic** range **that is** as high as possible. The analogous signal that is supplied to the second signal path...

...in an opposite direction in relation to the reinforced analogous signal (S2) in the first **signal path** (2, 3, 5). The differential amplification of the first and second signal path thus increases...

Claims:

...S1),the first and second analog part-signals (S2, S4) are each subjected to an **analog** -to- **digital conversion** (5, 6),the digitised part-signals (S5, S6) formed in this way are fed to a **digital** signal **processor** (**7**), or to digital circuits acting in an equivalent way, which processor generates the digital output...

...analog sub-signal;subjecting each of the first and second analog sub-signals to an **analog - to - digital conversion** to form first and second digitalized sub-signals, respectively; andapplying the first and second...

...off the second digitalized sub-signal in the digital signal processor and not utilizing the **second** digitalized **sub - signal** in forming the digital output signal when the second digitalized sub-signal has no useful ...

11/3,K/8 (Item 7 from file: 350)

0010792593 - Drawing available
WPI ACC NO: 2001-408094/200143
XRPX Acc No: N2001-301983

Broadband communication system e.g. for digitization and transport of broadband system return path signal, has transmitter which receives broadband signal having Gaussian distribution

Patent Assignee: SCIENTIFIC-ATLANTA INC (SCAT)
Inventor: FARHAN F M; QUESENBERRY P E

Patent Family (4 patents, 21 countries)

Patent Number	Kind	Application Date	Number	Kind	Date	Update
WO 2001035588	A2	20010517	WO 2000US29399	A	20001025	200143 B
BR 200015044	A	20020618	BR 200015044	A	20001025	200249 E
			WO 2000US29399	A	20001025	
US 6417949	B1	20020709	US 1999434267	A	19991105	200253 E
EP 1230773	A2	20020814	EP 2000986200	A	20001025	200261 E
			WO 2000US29399	A	20001025	

Priority Applications (no., kind, date): US 1999434267 A 19991105

Patent Details
Number Kind Lan Pg Dwg Filing Notes
WO 2001035588 A2 EN 13 2
National Designated States,Original: BR
Regional Designated States,Original: AT BE CH CY DE DK ES FI FR GB GR IE IT LU MC NL PT SE
BR 200015044 A PT PCT Application WO 2000US29399
Based on OPI patent WO 2001035588
EP 1230773 A2 EN PCT Application WO 2000US29399
Based on OPI patent WO 2001035588
Regional Designated States,Original: AT BE CH CY DE DK ES FI FR GB GR IE IT LI LU MC NL PT SE

Original Publication Data by Authority

Argentina

Assignee name & address:
Original Abstracts:
...digital signal. A receiving station (70), also located in the reverse path, receives the second **digital** signal, decodes the second digital signal to generate a third digital signal having a third...
...station (65) that receives a first analog signal, converts the first analog signal to a **first digital signal** having a first number of bits, encodes the first digital signal to generate a second...

...bits, then optically transmits the second digital signal. A receiving station (70), also located in **the** reverse **path** , receives the second digital signal, decodes the second **digital** signal **to** generate a third digital signal having a third number of bits greater than the second ...

...path includes a transmitting station (65) that receives a first analog signal, converts the first **analog** signal to a first digital signal having a first number of bits, encodes the first...

...path, receives the second digital signal, decodes the second digital signal to generate a third **digital** signal having a third number of bits **greater** than the second number of bits, then converts the third digital signal to a second...
Claims:

11/3,K/9 (Item 8 from file: 350)
DIALOG(R)File 350:Derwent WPIX

0009629798
WPI ACC NO: 1999-580939/199950
Related WPI Acc No: 1996-058019; 1996-069162; 1997-310145; 1998-130035; 1999-600286; 2000-095973; 2000-289404; 2000-442857; 2000-578505; 2001-181014; 2002-016847; 2002-327589; 2003-328056; 2003-415892; 2003-455960; 2004-032236; 2004-820135
XRPX Acc No: N1999-428984
Digital television signal receiver

Patent Assignee: SAMSUNG ELECTRONICS CO LTD (SMSU)
Inventor: LIMBERG A L; PATEL C B
Patent Family (14 patents, 9 countries)

Patent Number	Kind	Date	Application Number	Kind	Date	Update
AU 199887121	A	19990826	AU 199887121	A	19980930	199950 B
US 5966188	A	19991012	US 1996773949	A	19961226	199950 E
			US 199821946	A	19980211	
CN 1226117	A	19990818	CN 1998120772	A	19980929	199951 E
JP 11284932	A	19991015	JP 1998278812	A	19980930	200001 E
CA 2249035	A1	19990811	CA 2249035	A	19980929	200004 E
BR 199803857	A	19991214	BR 19983857	A	19980930	200016 E
AU 720014	B	20000518	AU 199887121	A	19980930	200032 E
KR 1999071401	A	19990927	KR 199840162	A	19980926	200048 E
MX 199808053	A1	19991001	MX 19988053	A	19980930	200103 E
US 6211924	B1	20010403	US 1996773949	A	19961226	200120 E
			US 199821946	A	19980211	
			US 1999415265	A	19991012	
KR 276772	B	20010115	KR 199840162	A	19980926	200206 E
SG 85096	A1	20011219	SG 19983424	A	19980904	200214 E
MX 199506	B	20001110	MX 19988053	A	19980930	200215 E
US RE38456	E	20040309	US 1996773949	A	19961226	200418 E
			US 199821946	A	19980211	
			US 2001973825	A	20011011	

Priority Applications (no., kind, date): US 1996773949 A 19961226; US 199821946 A 19980211; US 1999415265 A 19991012; US 2001973825 A 20011011

Alerting Abstract ...for synchrodyning an analog final intermediate-frequency output signal. The receiver portion also has an **A / D converter** for sampling and digitizing a signal, so that baseband signal is supplied from the receiver...

...A sample clock generator supplies a sample clock signal to time the sampling by the **A / D converter** . ...before performing channel equalization thereby reducing the number of samples in the kernels of the **digital** filters for performing **channel** equalization and substantially reduces the cost of the receiver.

Original Publication Data by Authority

Argentina

Assignee name & address:
Claims:
...resulting from said filtering and amplification to baseband thereby to generate a baseband signal; an **analog** -to- **digital converter** (**ADC**) included **in** said **radio receiver portion** for sampling one of said signals therein and digitizing it, so that said baseband signal...

...sample clock generator for supplying a sample clock signal to time the sampling by said **ADC** so that said first stream of digital **samples** has a sample rate substantially equal to a prescribed multiple MN times the symbol rate...

...of digital samples at a sample rate one Nth that of said first stream of **digital** samples; a **channel** equalizer for performing channel equalization on said second stream of **digital samples** to generate a channel equalizer response; and symbol decoding circuitry for decoding symbols in said...

...comprising: a radio receiver portion for selecting a channel for reception, for converting DTV signal **in** the selected **channel** to intermediate frequencies for filtering and amplification, and for synchrodyning an **analog** final intermediate-frequency output signal resulting from said filtering and amplification to baseband thereby to generate a baseband signal; an **analog - to - digital converter** (**ADC**) included in said radio receiver portion for sampling one of said signals therein and digitizing it, so that said **baseband** signal **is supplied from** said radio receiver portion as a first stream of digital samples descriptive of said baseband...

...sample clock generator for supplying a sample clock signal to time the sampling by said **ADC** so that said first stream of digital samples has a sample rate substantially equal to the symbol rate of said DTV signal as multiplied by **a** prescribed factor, which prescribed factor is more than one; an N:1 decimator connected for...
...rate one Nth that of said first stream of digital samples, N being a number **larger** than one; a channel equalizer for performing **channel** equalization on said second stream of digital samples to generate a channel equalizer response; and...

11/3,K/10 (Item 9 from file: 350)
DIALOG(R)File 350:Derwent WPIX

0008409744 - Drawing available
WPI ACC NO: 1997-526777/199748
Related WPI Acc No: 1997-526782; 1997-526783; 1997-526784
XRPX Acc No: N1997-438969
Communication system with bandwidth management for remote repeater network - forms signal within bandwidth of communication link via bandwidth management system which includes several mixing modes for performing signal conversion and reconstruction
Patent Assignee: JOHNSON CO E F (JOHN-N); TRANSCRYPT INT JOHNSON CO E F (TRAN-N)
Inventor: BAUMAN D R; DVORAK M D; JENSEN D J; LYON J K; PFIEFER S; PFIEFER S J; RUDE M J
Patent Family (6 patents, 73 countries)

Patent Number	Kind	Date	Application Number	Kind	Date	Update
WO 1997039535	A2	19971023	WO 1997US5985	A	19970411	199748 B
AU 199727263	A	19971107	AU 199727263	A	19970411	199809 E
WO 1997039535	A3	19971224	WO 1997US5985	A	19970411	199817 E
US 5896560	A	19990420	US 1996631866	A	19960412	199923 E
US 5991309	A	19991123	US 1996628981	A	19960412	200002 E
US 6049720	A	20000411	US 199615311	P	19960412	200025 E
			US 199627763	P	19961007	
			US 1997838853	A	19970411	

Priority Applications (no., kind, date): US 199615311 P 19960412; US 199615309 P 19960412; US 1996628981 A 19960412; US 1996630673 A 19960412; US 1996631866 A 19960412; US 199615309 A 19960412; US 199615311 A 19960412; US 199627763 P 19961007; US 199627763 A 19961007; US 1997838853 A 19970411

Original Publication Data by Authority

Argentina

Assignee name & address:
Claims:
...each of the one or more remote sites, controlling a transmitter, by the steps including: **analog** to **digital converting** the in-band tone **to** create **a digitized** in-band tone;detecting the digitized in-band tone using a processor;if the in...

...component are aligned in phase to a reference timing signal;receiving the gated signal at **a** remote site; **analog** to **digital converting** the gated signal to create a sequence of digitized samples, wherein the **analog to digital converting is** performed in phase with the reference timing signal;locating transition pairs in the sequence of...

...zero crossings associated with each of the transition pairs;averaging the zero crossings and using **the** averaged **value to** predict a starting point of the gated signal; andintroducing a delay **to** compensate **for a link** delay calculated from the starting point of the gated signal.

11/3,K/11 (Item 10 from file: 350)
DIALOG(R)File 350:Derwent WPIX

0007711640 - Drawing available
WPI ACC NO: 1996-334200/199633
XRPX Acc No: N1996-281608
Successive approximation analogue-digital converter for larger range input analog signals - has n-channel comparator and p-channel comparator allowing for larger range of analogue input signals to be converted into digital form
Patent Assignee: PSC INC (PSCP-N)
Inventor: COLEMAN E P
Patent Family (4 patents, 64 countries)
Patent Application
Number Kind Date Number Kind Date Update
WO 1996021281 A1 19960711 WO 1995US16401 A 19951229 199633 B
AU 199645211 A 19960724 AU 199645211 A 19951229 199644 E
US 5561427 A 19961001 US 1994366565 A 19941230 199645 E
US 5633641 A 19970527 US 1994366565 A 19941230 199727 E
US 1996582729 A 19960104

Priority Applications (no., kind, date): US 1994366565 A 19941230; US 1996582729 A 19960104

Original Titles:

Analog to **digital converter** with continuous conversion cycles and large input signal range...

... **Analog** to **digital converter** with continuous conversion cycles and large input signal range...

...LARGE INPUT **A / D CONVERTER** WITH CONTINUOUS CONVERSIONS

Original Publication Data by Authority

Argentina

Assignee name & address:
Original Abstracts:
A successive approximation A/D having dual comparators for allowing a larger range of analog **input** signals to **be converted** into **digital** form. **One** comparator **is** an N- **channel** device, and the other comparator is a P-channel device. The A/D switches to...

...approximating A/D having dual comparators for allowing a larger range of analog input signals **to be converted** into digital form. One comparator **is** an N- **channel** device (N39), and the other comparator **is** a P- **channel** device (N36). The A/D switches to either the N-channel device or the P...
Claims:
What is claimed is: A successive approximation **A / D converter** for receiving an analog **input signal and** outputting an n-bit digital signal, comprising:</br>means for receiving said analog input signal;</br>a digital-to- **analog converter** , said **digital** -to-analog **converter** including n input ports **for receiving** an **n** -bit **digital word** , and an output port for outputting an analog potential signal based on said n-bit...

11/3,K/12 (Item 11 from file: 350)
DIALOG(R)File 350:Derwent WPIX

0007709528 - Drawing available
WPI ACC NO: 1996-331935/199633
XRPX Acc No: N1996-280048
Clock signal reproduction circuit for regenerating clock signal from data recorded in opto-magnetic disk, optical disk - has analogue to digital converter to transform analogue signal into digital data according to clock pulse reproduced by voltage controlled oscillator
Patent Assignee: SONY CORP (SONY)
Inventor: KURA J; YOSHIMURA S
Patent Family (4 patents, 2 countries)

Patent Number	Kind	Date	Application Number	Kind	Date	Update
JP 8154053	A	19960611	JP 1994312190	A	19941215	199633 B
US 5802123	A	19980901	US 1994362808	A	19941222	199842 E
			US 1995552394	A	19951103	
US 5835544	A	19981110	US 1994362808	A	19941222	199901 E
JP 3458494	B2	20031020	JP 1994312190	A	19941215	200369 E

Priority Applications (no., kind, date): JP 1993328639 A 19931224; JP 1994229833 A 19940926

Alerting Abstract ...38) outputs a reproduction of a clock pulse contained in the received RF signal. The **ADC** receives the reproduced clock pulse from the VCO and uses the clock pulse to convert...

Original Publication Data by Authority

Argentina

Assignee name & address:
Original Abstracts:
A clock signal reproduction circuit including an **A / D conversion** circuit **for converting an** input RF analog signal with a restricted upper limit of a frequency band into a...

...calculation unit for digitally calculating a phase error of a digital signal converted in the **A / D conversion** circuit, **a control voltage** generating unit including a loop filter, **a D /A conversion unit for** outputting **an** analog control voltage signal based on the digital phase error calculated, and an analog voltage...

...a frequency of at least 2 times the frequency of the input analog signal. The **A / D conversion** circuit **uses the clock** signal output from the analog voltage-controlled type oscillating circuit to convert the input analog...
...A clock signal reproduction circuit including an **A / D conversion** circuit for converting an input RF **analog signal with** a restricted upper limit of a frequency band into a digital signal, a digital phase...

...calculation unit for digitally calculating a phase error of a digital signal converted in the **A / D conversion** circuit, a control voltage generating unit **including a loop** filter, **a D /A conversion** unit for outputting an analog **control voltage** signal **based** on the digital phase error calculated, and an analog voltage-controlled type oscillating circuit for...

...a frequency of at least 2 times the frequency of the input analog signal. The **A / D conversion** circuit uses the clock signal output **from the analog** voltage-controlled type oscillating circuit to convert the input analog signal into a digital format...
Claims:
...radio frequency (RF) signal which is encoded by a channel coding is equal to or **less** than 1/2 of a channel clock frequency of **digital** data to be reproduced, said **clock** signal reproduction circuit reproducing a clock signal from said analog input radio frequency (RF) signal, said clock signal reproduction circuit comprising:an **analog / digital conversion** circuit for converting said analog input radio frequency (RF) signal into a digital signal;digital **phase error calculation** means for digitally calculating a digital phase error of said digital signal converted in said **analog / digital conversion** circuit;control voltage generating means including a loop filter and digital/ **analog conversion** means **for** outputting an **analog control voltage** signal based on said digital phase error calculated;an **analog** voltage-controlled **type** oscillating **circuit** for outputting a reproduction clock signal having a frequency

equal to **said channel** clock frequency of said digital data to be reproduced, said **analog / digital conversion** circuit using said reproduction clock signal from said **analog** voltage- **controlled** type oscillating circuit to convert said analog input RF signal **into a digital** format;a first circuit havinga digital integration means for integrating said digital phase error...

...said digital phase error calculation means to produce a digital integration result,a first digital/ **analog conversion** circuit **for converting** said digital integration result into an analog signal, anda first coefficient multiplication circuit for multiplying with a converted result of said first digital/ **analog conversion circuit** a first coefficient; anda second circuit havinga **second digital** /analog **conversion** circuit for converting said digital phase error from said digital phase error calculation means into...

...a second coefficient multiplication circuit for multiplying with a converted result of said second digital/ **analog conversion circuit** a second coefficient, andan addition circuit for adding an output of the first circuit...

11/3,K/13 (Item 12 from file: 350)

0007188385 - Drawing available
WPI ACC NO: 1995-231764/199530
XRPX Acc No: N1995-180695
Mitigation of clipping effects in digital analog converter in echo canceller - coupling transmit signal on signal path to and derives received signal from bidirectional transmission path via hybrid circuit, with path operating on transmit signal which would normally introduce clipping
Patent Assignee: AMATI COMMUNICATIONS CORP (AMAT-N)
Inventor: BINGHAM J A C; CHOW J S; CIOFFI J M; FLOWERS M; FLOWERS M B
Patent Family (8 patents, 21 countries)

Patent Number	Kind	Date	Application Number	Kind	Date	Update
WO 1995017049	A1	19950622	WO 1994US13775	A	19941206	199530 B
AU 199512162	A	19950703	AU 199512162	A	19941206	199542 E
EP 734618	A1	19961002	WO 1994US13775	A	19941206	199644 E
			EP 1995904777	A	19941206	
US 5623513	A	19970422	US 1993165509	A	19931213	199722 E
AU 683332	B	19971106	AU 199512162	A	19941206	199802 E
JP 9510837	W	19971028	WO 1994US13775	A	19941206	199802 E
			JP 1995516790	A	19941206	
US 5787113	A	19980728	US 1993165509	A	19931213	199837 E
			US 1997789154	A	19970124	
KR 356383	B	20030114	WO 1994US13775	A	19941206	200339 E
			KR 1996703189	A	19960613	

Priority Applications (no., kind, date): US 1993165509 A 19931213; US 1997789154 A 19970124

Original Publication Data by Authority

Argentina

Assignee name & address:
Original Abstracts:
...coupled via a hybrid circuit to a bidirectional transmission path. The transmit path includes a **digital** -to- **analog converter** (DAC) having **a** given range **and** precision. **The** transmit **path** signal is limited and truncated to this range and precision before the DAC. In one...
Claims:
...digital signal range and/or digital precision which is less than that of the IFFT; **a** receive path including an **analog** -to- **digital converter** for **converting** a receive **signal** into **digital signal** samples **and** a Fast Fourier Transform (FFT) for transforming the receive signal samples from the time domain...

...or digital precision of the DAC, and wherein each input of the echo canceller from **the** transmit **path** is derived from the transmit path after the limiting and/or truncation unit...

...transmit signal comprising samples which are subject to clipping to a predetermined range by a **digital** - **to** -analog converter within the transmit path, the method comprising:scaling amplitudes of the transmit signal in accordance with the predetermined range prior **to** the **digital** -to- **analog converter** ;transmitting an indication of said scaling for complementary scaling at a receiver to which the...

11/3,K/14 (Item 13 from file: 350)
DIALOG(R)File 350:Derwent WPIX

0007023609 - Drawing available
WPI ACC NO: 1995-039684/199506
XRPX Acc No: N1995-031398
Signal processing device for digitised images - has digital signal processing part which processes signals converted by ADC **and output signal through DAC and uses buffers to exchange signals**
Patent Assignee: CANON KK (CANO)
Inventor: HIEDA T
Patent Family (3 patents, 2 countries)

Patent			Application			
Number	Kind	Date	Number	Kind	Date	Update
JP 6232744	A	19940819	JP 199313559	A	19930129	199506 B
US 6052021	A	20000418	US 1994186542	A	19940126	200026 E
			US 1996690344	A	19960726	
US 6285250	B1	20010904	US 1994186542	A	19940126	200154 E
			US 1996690344	A	19960726	
			US 2000527612	A	20000317	

Priority Applications (no., kind, date): JP 199313559 A 19930129

...has digital signal processing part which processes signals converted by ADC **and output signal through DAC and uses buffers to exchange signals**

Alerting Abstract ...has semiconductor IC (6) formed on a single semiconductor substrate. The IC comprises of an **ADC** (101), DAC (113,115), digital signal processing part (111) and analog signal processing parts. The...

Original Publication Data by Authority

Argentina

Assignee name & address:
Claims:
...first signals to and receiving second signals from said analog signal processing means through a **first path** and a second path, respectively, and for processing a **digital** signal, said first and second **paths** extending between said **analog** signal **processing** means and said digital signal processing means, said analog signal processing means and said digital...

...buffer means connected in said first path between said digital signal processing means and said **analog signal** processing means and second buffer means connected in **said** second **path** between said analog signal processing means and said **digital signal** processing means, said buffer means being constructed to prevent current which is greater than a...

...connected to said analog signal processing means through a predetermined path and for processing a **digital signal** , said predetermined **path** extending between said analog signal processing means and said **digital signal** processing means, said analog **signal** processing means and **said** digital signal processing means each including transistors which are formed on a commonsubstrate of said...

...signal processing means and said digital signal processing means, for preventing abnormal current which is **greater** than a predetermined magnitude from following through **said** predetermined **path** at least upon the application of power source voltages to said power supply wiring.

11/3,K/15 (Item 14 from file: 350)
DIALOG(R)File 350:Derwent WPIX

0005091279 - Drawing available
WPI ACC NO: 1990-077013/199011
Pseudo line locked clock for picture-in-picture video signals - uses available clock async. to incoming PIP video signals for acting as PIP memory write clock
Patent Assignee: N AMER PHILIPS CORP (PHIG); NORTH AMERICAN PHILIPS CORP (PHIG)
Inventor: JOHNSON L D
Patent Family (6 patents, 10 countries)

Patent Number	Kind	Date	Application Number	Kind	Date	Update
EP 358275	A	19900314	EP 1989202240	A	19890906	199011 B
FI 198904154	A	19900308			199022 E
JP 2113778	A	19900425	JP 1989227636	A	19890904	199023 E
US 4970596	A	19901113	US 1988241514	A	19880907	199048 E

EP 358275 B1 19930804 EP 1989202240 A 19890906 199331 E
DE 68908049 E 19930909 DE 68908049 A 19890906 199337 E
EP 1989202240 A 19890906

Priority Applications (no., kind, date): US 1988241514 A 19880907
Patent Details
Number Kind Lan Pg Dwg Filing Notes
EP 358275 A EN 8 4
Regional Designated States,Original: AT BE DE FR GB IT
EP 358275 B1 EN 11 4
Regional Designated States,Original: AT BE DE FR GB IT NL
DE 68908049 E DE Application EP 1989202240
Based on OPI patent EP 358275

Equivalent Alerting Abstract ...In the appts. the write clock controlling operation of the PIP circuitry (e.g. the **analog digital converter** in the PIP channel) utilises a clock signal source having a substantially higher frequency (preferably...

Original Publication Data by Authority

Argentina

Assignee name & address:
Original Abstracts:
...The write clock controlling operation of the PIP circuitry (e.g. the **analog digital converter in the PIP channel**) utilizes a clock signal source having a substantially **higher** frequency (preferably six times) the desired write clock frequency. This clock signal is applied to ...
Claims:

11/3,K/16 (Item 15 from file: 350)
DIALOG(R)File 350:Derwent WPIX
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0002856444
WPI ACC NO: 1983-G0352K/198318
XRPX Acc No: N1983-078777
Acoustic equipment for geological mapping of ocean bed - has simultaneously operating A - D conversion **channels to give data on cross-section of deposits**
Patent Assignee: LENINGRAD PLEKHANOV MINE (LEMI)
Inventor: SVECHNIKOV A I
Patent Family (1 patents, 1 countries)
Patent Application
Number Kind Date Number Kind Date Update
SU 938232 B 19820627 SU 3265901 A 19810323 198318 B

Patent Details
Number Kind Lan Pg Dwg Filing Notes
SU 938232 B RU 7 3

...has simultaneously operating A - D conversion **channels to give data**

on cross-section of deposits
Alerting Abstract ...computer analysis of the structure and lithology of ocean bed deposits. The use of independent **analog - digital conversion channels** widens the echo signal recording range towards **higher** frequencies...

...a 3rd timer (7) to form the recording intervals for the different channels of an **analog - digital converter** (10...

Original Publication Data by Authority

Argentina
?

13/3,K/1 (Item 1 from file: 350)
DIALOG(R)File 350:Derwent WPIX

0015323522 - Drawing available
WPI ACC NO: 2005-673771/200569
XRPX Acc No: N2005-552507
Traveling wave multiplying digital-to-analog converter for e.g. satellite, has cells linked to local oscillator transmission line, and output transmission line on which output with differential output current is provided
Patent Assignee: BOEING CO (BOEI)
Inventor: HITKO D
Patent Family (2 patents, 1 countries)

Patent Number	Kind	Date	Application Number	Kind	Date	Update
US 20050200508	A1	20050915	US 2004796629	A	20040308	200569 B
US 6952177	B1	20051004	US 2004796629	A	20040308	200569 E

Priority Applications (no., kind, date): US 2004796629 A 20040308

Patent Details

Number	Kind	Lan	Pg	Dwg	Filing Notes
US 20050200508	A1	EN	16	7	

Alerting Abstract ...a method for digital-to- **analog conversion a** communication system **comprising** a traveling wave multiplying digital-to-analog converter...

Original Publication Data by Authority

Argentina

Assignee name & address:
Original Abstracts:
A traveling wave multiplying digital-to- **analog** converter **has** propagation- **delay matched** transmission **lines** for **conversion** of a high data rate digital input to a high frequency RF analog output, for example, at microwave and millimeter wave frequencies and above. The traveling wave multiplying digital-to- **analog converter includes** an array **of** constant, high impedance multiplying cells that are identical to improve component matching and propagation delay...

...bandwidth digital input. The interleaving effects a "spatial averaging" that maintains linearity of digital to **analog conversion in** the presence **of** any linear gradient delta from one cell to another across the array of multiplying cells...

...A traveling wave multiplying digital-to-analog converter has propagation-delay **matched** transmission **lines** for conversion of a high data **rate digital input** to a high frequency RF analog output, for example, at microwave and millimeter wave frequencies...

...are connected in a spatial interleaving manner along bit lines that propagate the high bandwidth **digital** input. The **interleaving** effects a "spatial averaging" that maintains linearity of digital to analog conversion in the presence...
Claims:
1. A multiplying digital-to- **analog converter comprising** :a plurality **of** multiplying cells, wherein each multiplying cell is connected to a differential local oscillator bias signal...

13/3,K/2 (Item 2 from file: 350)
DIALOG(R)File 350:Derwent WPIX

0015229874 - Drawing available
WPI ACC NO: 2005-579938/200559
XRPX Acc No: N2005-475681
Analog **to** digital converting **apparatus for monitoring system, has notifying units outputting signal notifying that channel`s digital data exceeds its threshold, and units holding data required to analyze cause of threshold excess**
Patent Assignee: FUJITSU LTD (FUIT)
Inventor: SAITO H
Patent Family (2 patents, 2 countries)

Patent Number	Kind	Date	Application Number	Kind	Date	Update
US 6930629	B1	20050816	US 2004947365	A	20040923	200559 B
JP 2005333258	A	20051202	JP 2004148093	A	20040518	200579 E

Priority Applications (no., kind, date): JP 2004148093 A 20040518

Patent Details

Number	Kind	Lan	Pg	Dwg	Filing Notes
US 6930629	B1	EN	12	5	
JP 2005333258	A	JA	12		

Analog **to** digital converting **apparatus for monitoring system, has notifying units outputting signal notifying that channel`s digital data...**

Original Titles:
Analog / digital converting apparatus

Alerting Abstract ...NOVELTY - The apparatus has notifying units (20) externally outputting a signal notifying that **digital** data of **channels** exceeds its threshold, to an external device. The notifying units keeps sending the signal until...

...a comparing unit which compares, in sequence, the individual channels of digital data obtained by **analog / digital converter** .
...

...DESCRIPTION OF DRAWINGS - The drawing shows a block diagram showing a construction of an **A / D** (**analog / digital**) **converting** apparatus...

...10 **A / D converting** apparatus

Original Publication Data by Authority

Argentina

Assignee name & address:
Original Abstracts:
Upon detection of any abnormality in digital data of one **of** the input **channels** , it is possible to read, with reliability, digital data of all **the** remaining **channels** whose conversion is performed after conversion of the one channel. The apparatus includes: a comparing units which sequentially **compares** individual channels of **digital** data **obtained** by the **analog / digital converter** to **thresholds associated** , **one** with each of the channels; a **digital** data **holding** units which holds, if the **comparing** units detects that **one** of the channels of **digital** data **exceeds** its associated threshold, digital data of the **one channel** and also **digital data** of the **remaining channels** whose conversion is performed after conversion of the one channel; and a notifying units which externally outputs a signal notifying that the digital data of the **one channel** exceeds its associated threshold the moment the digital data holding units **stores** all the **channels** of **digital** data.
Claims:
1. An **analog / digital converting apparatus** , **comprising** :an **analog / digital converter** which **converts in sequence** a **plurality** of channels of **analog** data, **which** is externally input to the apparatus, into a plurality of channels of **digital** data; **comparing** units which **compares** , in sequence, **the** individual channels **of digital** data obtained by **said analog / digital converter** to thresholds associated, **one with each** of the **channels** ;digital data holding units which holds, if said comparing units detects that one of the channels of digital data exceeds its associated threshold, **digital** data **of** the one **channel** and also digital data of the remaining channels whose conversion is performed after conversion of...

...the digital data of the one channel exceeds its associated threshold the moment when said **digital data** holding units holds all the channels of digital data.

13/3,K/3 (Item 3 from file: 350)
DIALOG(R)File 350:Derwent WPIX

0014792004 - Drawing available
WPI ACC NO: 2005-139688/200515
XRPX Acc No: N2005-118789
Data acquisition, processing and transmitting unit of locomotive
Patent Assignee: UNIKAM STOCK CO (UNIK-R)

Inventor: SARKISOV A L; SLESAREV S N; VLASOV V V
Patent Family (1 patents, 1 countries)
Patent Application
Number Kind Date Number Kind Date Update
RU 2242380 C1 20041220 RU 2003112985 A 20030506 200515 B

Priority Applications (no., kind, date): RU 2003112985 A 20030506

Patent Details
Number Kind Lan Pg Dwg Filing Notes
RU 2242380 C1 RU 0 1

Alerting Abstract ...NOVELTY - Matching device installed in housing is provided with connectors and **digital channels** for connecting discrete signals pickups, being connected to central processor. The processor, designed for processing...
DESCRIPTION - **Matching** device is furnished with **analog channels** to connect analogue signal pickups and **analog** -to- **digital converters** . Central processor is provided with flash memory and it includes additionally software for calibrating of **analog channels** . Serial port transceiver is designed for interaction of **analog channels** calibration program with corresponding terminals or PC-compatible computer. The latter is provided with terminal...

Original Publication Data by Authority

Argentina

13/3,K/4 (Item 4 from file: 350)
DIALOG(R)File 350:Derwent WPIX

0010534997 - Drawing available
WPI ACC NO: 2001-137476/200114
XRPX Acc No: N2001-100152
Analog front end for communications system, includes summing amplifier which adds the output signal of hybrid with output signal of attenuator along AES path to produce echo-cancelled receive signal
Patent Assignee: EXCESS BANDWIDTH CORP (EXCE-N); VIRATA CORP (VIRA-N)
Inventor: CHARI S; HANSEN C; LU C; PAL D
Patent Family (4 patents, 91 countries)
Patent Application
Number Kind Date Number Kind Date Update
WO 2000059124 A1 20001005 WO 2000US8115 A 20000324 200114 B
AU 200040351 A 20001016 AU 200040351 A 20000324 200114 E
EP 1163732 A1 20011219 EP 2000919709 A 20000324 200206 E
WO 2000US8115 A 20000324
US 6542477 B1 20030401 US 1999281903 A 19990331 200324 E

Priority Applications (no., kind, date): US 1999281903 A 19990331

Patent Details
Number Kind Lan Pg Dwg Filing Notes
WO 2000059124 A1 EN 19 7
National Designated States,Original: AE AG AL AM AT AU AZ BA BB BG BR BY

CA CH CN CR CU CZ DE DK DM DZ EE ES FI GB GD GE GH GM HR HU ID IL IN IS JP KE KG KP KR KZ LC LK LR LS LT LU LV MA MD MG MK MN MW MX NO NZ PL PT RO RU SD SE SG SI SK SL TJ TM TR TT TZ UA UG UZ VN YU ZA ZW
Regional Designated States,Original: AT BE CH CY DE DK EA ES FI FR GB GH GM GR IE IT KE LS LU MC MW NL OA PT SD SE SL SZ TZ UG ZW
AU 200040351 A EN Based on OPI patent WO 2000059124
EP 1163732 A1 EN PCT Application WO 2000US8115
Based on OPI patent WO 2000059124
Regional Designated States,Original: AL AT BE CH CY DE DK ES FI FR GB GR IE IT LI LT LU LV MC MK NL PT RO SE SI

Alerting Abstract ...the hybrid to the output signal of a digitally-controlled attenuator (217) provided at an **analog** echo synthesis **path** to produce an echo-cancelled receive signal.

Original Publication Data by Authority

Argentina

Assignee name & address:
Original Abstracts:
...especially useful in a High-bit-rate Digital Subscriber Line (HDSL) or HDSL.2 environment. An **analog** echo simulation **path** **is** provided capable **of** simulating echo from a wide variety of echo paths. Digitally controlled attenuators are provided in the transmission path and in the **analog** echo simulation **path** . **Also** provided is **a** digital-tunable equalizer stage. The equalizer stage is tuned to match the characteristics of the...

...especially useful in a High-bit-rate Digital Subscriber Line (HDSL) or HDSL.2 environment. An **analog** **echo** simulation **path** is provided capable of simulating echo from a **wide** variety of **echo** **paths** . Digitally controlled attenuators are provided in the transmission path and in the **analog** echo simulation **path** . Also provided is a **digital** -tunable equalizer stage. **The** equalizer stage **is** tuned to **match** the **characteristics** of the receive **path** . The same arrangement may be **adapted** for various DSL technologies, i.e., xDSL. There results an analog front end that is...

...especially useful in a High-bit-rate Digital Subscriber Line (HDSL) or HDSL.2 environment. An **analog** echo simulation **path** is provided capable of simulating echo from a wide variety of echo paths. **Digitally** controlled attenuators **are** provided in the transmission path and in the **analog** echo simulation **path** . **Also** provided is a digital-tunable equalizer stage. The equalizer stage is tuned **to** **match** the **characteristics** of the receive path. The same arrangement may be adapted for various DSL technologies, **i** .e., xDSL. There results an **analog** front end that is well-adapted to high-speed wireline communications...
Claims:
...a transmit signal provided to the communication hybrid, the transmit path unit including a first **digital** to **analog** converter **and** a first digitally-tunable **analog** attenuator;at **least** one echo cancellation signal path unit producing an echo cancellation signal, the echo cancellation path unit including a second digital to **analog** converter and a **second** digitally-tunable **analog** attenuator; **and** means for **summing** the echo cancellation signal together with a received signal from the

communications hybrid to produce...

13/3,K/5 (Item 5 from file: 350)
DIALOG(R)File 350:Derwent WPIX

0010104942 - Drawing available
WPI ACC NO: 2000-412105/200035
Related WPI Acc No: 1998-110277
XRAM Acc No: C2000-124895
XRPX Acc No: N2000-308067
Oximeter for non-invasively measuring arterial oxygen saturation provides direct digital signals from input signals produced by sensor connected to oximeter
Patent Assignee: CRITICARE SYSTEMS INC (CRIT-N); LARSEN M T (LARS-I); REUSS J L (REUS-I)
Inventor: LARSEN M T; REUSS J L
Patent Family (11 patents, 25 countries)

Patent Number	Kind	Application Date	Number	Kind	Date	Update
WO 2000032099	A1	20000608	WO 1999US28452	A	19991201	200035 B
AU 200018393	A	20000619	AU 200018393	A	19991201	200044 E
US 6163715	A	20001219	US 1996683617	A	19960717	200102 E
			US 1998201942	A	19981201	
US 20010005773	A1	20010628	US 1996683617	A	19960717	200138 E
			US 1998201942	A	19981201	
			US 2000740595	A	20001219	
EP 1146812	A1	20011024	EP 1999961905	A	19991201	200171 E
			WO 1999US28452	A	19991201	
CN 1335756	A	20020213	CN 1999813986	A	19991201	200233 E
BR 199915798	A	20020604	BR 199915798	A	19991201	200246 E
			WO 1999US28452	A	19991201	
JP 2003505115	W	20030212	WO 1999US28452	A	19991201	200321 E
			JP 2000584802	A	19991201	
US 6526301	B2	20030225	US 1996683617	A	19960717	200323 E
			US 1998201942	A	19981201	
			US 2000740595	A	20001219	
AU 770773	B2	20040304	AU 199738029	A	19970717	200453 E
			AU 200018393	A	19991201	
CN 1198534	C	20050427	CN 1999813986	A	19991201	200641 E

Priority Applications (no., kind, date): US 1996683617 A 19960717; US 1998201942 A 19981201; US 2000740595 A 20001219

Alerting Abstract ...range control to adjust the range of the signal to an expected input range, an **analog** to **digital converter** , **and a** processing unit to process the voltage signal generated to calculate the arterial oxygen saturation; non...

...skinned patients. There is a reduction in potential errors by processing all signals along one **digital** hardware **path** to eliminate the need for **matched analog components** . The oximeter has a reduced **number** of electronic components. The apparatus is small and cheap to operate...

Original Publication Data by Authority

Argentina

Assignee name & address:
Claims:
...producing an analog electrical current signal representing the absorption of each wavelength of said light; **an analog** to **digital converter** for **converting** said analog electrical current signal to a digital voltage **signal** ; and **a processing** unit **for** processing said digital voltage signal to calculate an arterial oxygen saturation...

...blood oxygenation level if the signal is below the predetermined range; andfirst reducing the **analog** current **signal** and **converting** the reduced analog current signal to a reduced digital voltage signal and then analyzing the...

13/3,K/6 (Item 6 from file: 350)
DIALOG(R)File 350:Derwent WPIX

0008458892 - Drawing available
WPI ACC NO: 1997-335238/199731
XRPX Acc No: N1997-278120
Digital centre line filter for filtering all but single line at centre frequency of frequency spectrum - has digital filter for processing digital converter signals to which weighting device applies complex weights, and decimation processor for processing digital filter output by set factor
Patent Assignee: HUGHES MISSILE SYSTEMS CO (HUGA); RAYTHEON CO (RAYT)
Inventor: TARGOFF D M
Patent Family (13 patents, 12 countries)

Patent Number	Kind	Date	Application Number	Kind	Date	Update
EP 782259	A2	19970702	EP 1996309476	A	19961224	199731 B
NO 199605567	A	19970627	NO 19965567	A	19961223	199736 E
AU 199676514	A	19970724	AU 199676514	A	19961224	199737 E
US 5661487	A	19970826	US 1995578800	A	19951226	199740 E
CA 2193435	A	19970627	CA 2193435	A	19961219	199743 E
JP 9325181	A	19971216	JP 1996346036	A	19961225	199809 E
AU 703191	B	19990318	AU 199676514	A	19961224	199923 E
CA 2193435	C	19990727	CA 2193435	A	19961219	199949 E
IL 119898	A	20001031	IL 119898	A	19961224	200059 E
EP 782259	B1	20030514	EP 1996309476	A	19961224	200333 E
DE 69628130	E	20030618	DE 69628130	A	19961224	200348 E
			EP 1996309476	A	19961224	
ES 2198467	T3	20040201	EP 1996309476	A	19961224	200414 E
NO 319892	B1	20050926	NO 19965567	A	19961223	200565 E

Priority Applications (no., kind, date): US 1995578800 A 19951226; EP 1996309476 A 19961224

Alerting Abstract ...to pulse repetition frequency to filter received pulsed signal to provide an analog filter signal, **analog - digital converter** (56A) responsive to analog filter signals for conversion to digital signals and digital filter (58A...

Original Publication Data by Authority

Argentina

Assignee name & address:
Original Abstracts:
...spectrum. The signal is passed through the analog filter, and then over-sampled by an **analog** -to- **digital convertor** (**56A**). A **sharp cutoff** FIR filter is used as the digital filter (58A) to **eliminate** the remaining undesired **lines** , since the **analog filter** already has the correct **matched** filter characteristic in the passband, the digital filter passband is deliberately wider and unsymmetrical. After...
Claims:
...to the PRF for filtering the received pulsed signal to provide an analog filter signal;</br> **analog** -to- **digital convertor** (56A) responsive to the **analog filter** signal **for converting** the analog filter signal **to** a **digital convertor signal** , the convertor sampling the **analog** filter **signal at** a high rate in comparison to the PRF;</br> a digital filter (58A) for processing the...

...including weighting means for applying complex weights to the digital convertor signals; and</br> wherein the **analog** filter and **digital** filter act **in** combination to provide a filter having a composite filter response characteristic which provides a narrow...

...to-noise ratio, for filtering the received pulsed signal to provide an analog filter signal; **analog** -to- **digital convertor** (56A) responsive to the analog filter signal for converting the analog filter **signal** to a **digital convertor** signal, the convertor sampling the analog filter signal at a high rate in comparison to...

...a digital filter (58A) for processing the digital convertor signals, the digital filter including weighting **means** for **applying complex** weights to the digital convertor signals; andwherein the analog filter and digital filter act...pulsed signal to provide an analog filter signal, said filter having an analog filter passband; **analog** -to- **digital convertor** responsive to the analog filter signal for converting the analog filter signal to a digital...

...convertor signals, the digital filter including weighting means for applying complex weights to the digital **convertor** signals, **said digital** filter providing a sharp cutoff filter which eliminates all **unwanted** spectral **lines** ; andwherein the **analog** filter and **digital** filter act in combination to provide a filter having a composite filter response characteristic which...

^ 13/3,K/7 (Item 7 from file: 350)

0007594365 - Drawing available
WPI ACC NO: 1996-211434/199622
XRPX Acc No: N1996-176924
Calibrating channel gain within multichannel analog device - trimming with precision at manufacture first reference channel which is used by digital processing circuitry as reference for channel gain calibration
Patent Assignee: AMERICAN TELEPHONE & TELEGRAPH CO (AMTT); AT & T CORP (AMTT); LUCENT TECHNOLOGIES INC (LUCE)
Inventor: MARSH D G; VAIDEN R H
Patent Family (4 patents, 6 countries)

Patent		Application			
Number	Kind	Date	Number	Kind	Date	Update
EP 709968	A1	19960501	EP 1995307431	A	19951018	199622 B
JP 8279720	A	19961022	JP 1995299287	A	19951025	199701 E
TW 283282	A	19960811	TW 1995109431	A	19950908	199701 E
US 5596322	A	19970121	US 1994329590	A	19941026	199710 E

Priority Applications (no., kind, date): US 1994329590 A 19941026

Original Publication Data by Authority

Argentina

Assignee name & address:
Original Abstracts:
A method and structure for automatically calibrating various paths within multi-channel **analog** integrated circuits is disclosed. The invention calls for digital signal processing circuitry to correct for...

...A method and structure for automatically calibrating various paths within multi-channel **analog** integrated **circuits** is disclose. The invention calls for digital signal processing circuitry to correct for absolute gain...

...first reference channel is precision trimmed at manufacture and used by the digital processing circuitry **as** a reference for **channel** gain calibration. When the circuit is powered for use, the other channels are calibrated based...
Claims:
1. A method of calibrating channel gain within a multi-channel **analog device** , **said** device comprising N **channels** and including control circuitry for controlling a gain of each said N channels, comprising the...

...Claim 16. A codec comprising N channels, wherein each of said N channels includes an **analog** to **digital** (**A / D**) **conversion path** having a first **analog amplifier** in series **with** an **A / D converter** , **and a** digital to **analog** (**D** /A) conversion **path** having **a D / A converter** in series with a **second analog** amplifier, and **wherein** a **gain of** one **of** said A/D paths has been calibrated by trimming during codec fabrication, said codec further comprising: a) **analog** means for providing an analog calibration signal to each said N A/D paths; b) first **comparing** means for **comparing** (**N** -1) A/D **path** output signals generated within (N-1) corresponding ones of said non-calibrated A/D paths ...

...response to said analog calibration signal, wherein A/D gain correction coefficients are determined; c) **digital means** for providing a digital calibration signal to each said N D/A paths; d) loopback means for providing **analog** D/A **path** output signals generated in each said N D/A paths in response to said digital calibration signal, respectively, **to** at least **one** of said N A/D paths; and e) second comparing means for comparing N digital...

13/3,K/8 (Item 8 from file: 350)
DIALOG(R)File 350:Derwent WPIX

0006163830 - Drawing available
WPI ACC NO: 1992-407311/199249
XRPX Acc No: N1992-310619
Self calibrating dual range A **-** D converter **- has gain matchin**g circuit **balancing upper end of level-dependent dual signal path transfer curves, and** digital **comparator evaluating respective** path **codewords**
Patent Assignee: EASTMAN KODAK CO (EAST)
Inventor: BERNSTEIN L J; MEAD T W
Patent Family (8 patents, 19 countries)

Patent Number	Kind	Application Date	Number	Kind	Date	Update
US 5164726	A	19921117	US 1991715092	A	19910612	199249 B
WO 1992022962	A1	19921223	WO 1992US4862	A	19920608	199302 E
AU 199222363	A	19930112	AU 199222363	A	19920608	199317 E
EP 542995	A1	19930526	EP 1992913566	A	19920608	199321 E
			WO 1992US4862	A	19920608	
AU 643394	B	19931111	AU 199222363	A	19920608	199401 E
JP 6500907	W	19940127	WO 1992US4862	A	19920608	199409 E
			JP 1993500987	A	19920608	
EP 542995	B1	19960417	EP 1992913566	A	19920608	199620 E
			WO 1992US4862	A	19920608	
DE 69209974	E	19960523	DE 69209974	A	19920608	199626 E
			EP 1992913566	A	19920608	
			WO 1992US4862	A	19920608	

Priority Applications (no., kind, date): US 1991715092 A 19910612

Self calibrating dual range A **-** D converter **- ...**

...gain matching circuit balancing upper end of level-dependent dual signal path transfer curves, and digital **comparator evaluating respective** path **codewords**

Original Titles:
...SELF CALIBRATING DUAL RANGE **A / D CONVERTER**
...

...SELF CALIBRATING DUAL RANGE **A / D CONVERTER**
...
...Self calibrating dual range **A / D converter**
...

...SELF CALIBRATING DUAL RANGE **A / D CONVERTER**

Alerting Abstract ...The dual range **analog** -to- **digital converter** has two signal paths, each having a respective **analog** -to- **digital converter** producing respective first and second digital signals. A gain device provides signal gain in the...

Original Publication Data by Authority

Argentina

Assignee name & address:
Original Abstracts:
A dual range **A / D converter includes** a gain matching circuit (60) for balancing the upper end of the transfer curves of...

...gain path A). A digital comparator (62) compares the digital code word output of flash **A / D converters** (**12** , 10) included in the respective paths, with the output from the high gain path being...

...which equalizes the lower end of the transfer curves,a fully self-calibrating dual range **A / D converter is** obtained...

...A dual range **A / D converter includes a gain** matching circuit for balancing the upper end of the transfer curves of the level-dependent dual A/D signal **paths of** the **converter** so as to control crossover between the paths. One path (high gain path) is provided...
...is a nominal multiple of gain applied to the other path (low gain path). A **digital comparator compares** the digital **code** word output of flash **A / D converters included in the** respective paths, with the output from the high gain path being scaled down to correspond...

...which equalizes the lower end of the transfer curves, a fully self-calibrating dual range **A / D converter is obtained** .

...

...A dual range **A / D converter** includes a **gain matching circuit** (60) for balancing the upper end of the transfer curves of the level-dependent dual A/D signal paths of **the converter** so as to control crossover between the paths. One path (high gain path B) is...

...a nominal multiple of gain applied to the other path (low gain path A). A **digital** comparator (**62**) **compares** the digital code word **output** of flash **A / D converters** (12, 10) **included in the** respective paths, with the output from the high gain path being scaled down to correspond...

...which equalizes the lower end of the transfer curves,a fully self-calibrating dual range **A / D converter** is obtained.
Claims:
The dual range **analog** -to- **digital converter** has two signal paths, each having a respective **analog** -to- **digital converter** producing respective first and second digital signals. A gain device provides signal gain in the ...

...A dual range **analog** -to- **digital converter** for **converting** analog input signals **into digital output signals** , the **digital** signals having code values corresponding to the analog levels of the input signals, said converter comprising **a** first signal **path** (A) including a first **analog** -to- **digital converter** (**10**) for converting the **analog input** signals **into first** coded value digital signals, **a** second signal **path** (B) including a second **analog** -to- **digital converter** (**12**) for converting the **analog input** signals **into second** coded value digital signals, means (14, 16) for providing signal gain **in** the respective signal **paths** , the gain applied to the second path being a nominal multiple of the gain applied...

...respective signal paths for generating the digital output signals from either the first signal path **or** the second signal **path** ,said dual range converter further characterized by: evaluating means including a digital comparator (60) for comparing the code values of the digital signals from the respective **analog** -to- **digital converters** , the code values in one of **the paths being scaled** with respect to the code values in the other path to account for the nominal...

13/3,K/9 (Item 9 from file: 350)

0002518755
WPI ACC NO: 1982-F0417E/198218
Digital telecommunications circuit - matches impedances between analogue and digital subscribers using low power integrated circuits
Patent Assignee: ALCATEL NV (ALCA-N); INT STANDARD ELECTRIC CORP (INTT)
Inventor: ROSEWOON J; TREIBER R
Patent Family (87 patents, 21 countries)

Patent Number	Kind	Application Date	Number	Kind	Application Date	Update
BE 890839	A	19820423	BE 890839	A	19811023	198218 B
GB 2086196	A	19820506	GB 198128572	A	19810922	198218 E
GB 2086197	A	19820506	GB 198128571	A	19810922	198218 E
GB 2086198	A	19820506	GB 198128569	A	19810922	198218 E
NO 198103437	A	19820518			198223	E
NO 198103438	A	19820518			198223	E
NO 198103439	A	19820518			198223	E
NO 198103440	A	19820518			198223	E
SE 198106156	A	19820524			198223	E
SE 198106157	A	19820524			198223	E
SE 198106158	A	19820524			198223	E
SE 198106159	A	19820524			198223	E
FR 2493078	A	19820430			198224	E
FR 2493080	A	19820430			198224	E
FR 2493082	A	19820430			198224	E
FR 2493083	A	19820430			198224	E
NL 198104701	A	19820517			198224	E
NL 198104702	A	19820517			198224	E
NL 198104731	A	19820517			198224	E
NL 198104732	A	19820517			198224	E
DE 3141501	A	19820624	DE 3141502	A	19811020	198226 E
DK 198104658	A	19820607			198226	E

DK 198104659 A 19820607 198226 E
DK 198104660 A 19820607 198226 E
DK 198104661 A 19820607 198226 E
DE 3141500 A 19820701 DE 3141503 A 19811020 198227 E
BR 198106624 A 19820629 198228 E
BR 198106686 A 19820629 198228 E
PT 73847 A 19820608 198228 E
PT 73848 A 19820608 198228 E
PT 73849 A 19820608 198228 E
PT 73850 A 19820608 198228 E
BR 198106756 A 19820706 198229 E
BR 198106781 A 19820706 198229 E
FI 198103326 A 19820630 198229 E
FI 198103327 A 19820630 198229 E
FI 198103328 A 19820630 198229 E
FI 198103329 A 19820630 198229 E
JP 57099828 A 19820621 198230 E
JP 57099829 A 19820621 198230 E
JP 57099830 A 19820621 198230 E
DE 3141502 A 19820729 DE 3141501 A 19811020 198231 E
JP 57103438 A 19820628 198231 E
DE 3141503 A 19820708 DE 3141503 A 19811020 198239 E
US 4351060 A 19820921 US 1980199806 A 19801023 198240 E
US 1980199904 A 19801023
US 1980199906 A 19801023
ZA 198106775 A 19820825 198247 E
ZA 198106777 A 19821130 198308 E
ZA 198106778 A 19821130 198308 E
ZA 198106780 A 19821130 198308 E
US 4377858 A 19830322 US 1980199806 A 19801023 198314 E
US 1980199905 A 19801023
US 1980199906 A 19801023
GB 2107554 A 19830427 198317 E
US 4381561 A 19830426 US 1980199806 A 19801023 198319 E
US 1980199906 A 19801023
US 4386430 A 19830531 US 1980199806 A 19801023 198324 E
US 1980199906 A 19801023
ES 198401293 A 19840216 198423 E
CA 1165823 A 19840417 198426 E
IL 63995 A 19840430 198426 E
CA 1168775 A 19840605 198427 E
CA 1168776 A 19840605 198427 E
CA 1168777 A 19840605 198427 E
GB 2107554 B 19840801 198431 E
IL 64020 A 19840930 198445 E
GB 2086197 B 19841205 198449 E
GB 2086198 B 19841205 198502 E
IL 63994 A 19841031 198506 E
RO 84855 A 19840930 198510 E
RO 84856 A 19840930 198510 E
RO 84864 A 19840930 198510 E
RO 84896 A 19840930 198510 E
IL 63993 A 19850331 198517 E
IL 72814 A 19850331 198517 E
GB 2086196 B 19850501 198518 E
CH 656271 A 19860613 198630 E

CH 656272	A	19860613			198630	E	
CH 656267	A	19860617			198634	E	
CH 656759	A	19860715			198634	E	
DE 3141502	C	19880114	DE 3141502	A	19811020	198802	E
DE 3141503	C	19880121	DE 3141503	A	19811020	198803	E
DE 3141501	C	19880128	DE 3141501	A	19811020	198804	E
SE 456062	B	19880829			198837	E	
IT 1195220	B	19881012			199108	E	
IT 1195221	B	19881012			199108	E	
IT 1195222	B	19881012			199108	NCE	
IT 1195223	B	19881012			199108	E	
AT 198104511	A	19910815			199136	NCE	
AT 198104512	A	19910815			199136	E	
AT 198104514	A	19910815			199136	E	
NL 191663	B	19950801	NL 19814702	A	19811016	199537	E

Priority Applications (no., kind, date): US 1980199806 A 19801023; US 1980199904 A 19801023; US 1980199905 A 19801023; US 1980199906 A 19801023

Original Titles:
...All digital LSI line circuit for **analog lines**

Alerting Abstract ...This automatic digital synthesiser is used for **matching** two-wire analogue and **digital** telephone subscriber **lines** with four-line trunk lines using integrated circuits. Conversion from two-wire to four-wire...

Equivalent Alerting Abstract ...The telephone circuit arrangement has an A / D **converter** (135) in the four-wire receive path to convert the analog signal from the telephone line (102,104) into a digital signal. **A** D /A **converter** (114) in the four-wire transmit path does the reverse. A digital summation circuit (151) in the four-wire transmit path adds the digital output of the **A / D converter** as negative feedback to the digital transmit signal from the digital exchange...

...resistance of the converter to the apparent resistance of the telephone subscriber line via an **A / D converter** in the 2-wire path, or D/A converter in the 4-wire path and a digital filter coupled to a summing circuit combinging the digital output of the **A / D converter** (135) with the incoming digital signal from the digital exchange...

...An **A / D converter** in the four-wire reception path converts the two-wire analog signal to digital, and **a D** /A **converter** in the send path converts outgoing data. A digital filter is fed with send data...

...output impedance, and a digital summer combines the output of the first filter with the **A / D converter** output to compensate for echoes arising from the send signal. (26pp)N

Original Publication Data by Authority

Argentina

Assignee name & address:

Claims:
...A circuit for automatically digitally synthesizing an output matching line terminating impedance including: (**a**) analog **to digital** conversion means for converting analog communication signals occurring at circuit output terminals to digital signals...

...impedance such that said analog current is coupled to said circuit output terminals and to **said** analog **to digital** conversion means.a

...

14/3,K/1 (Item 1 from file: 350)
DIALOG(R)File 350:Derwent WPIX

0017156729 - Drawing available
WPI ACC NO: 2007-871677/200780
Related WPI Acc No: 2002-381487; 2002-566313; 2003-057466; 2008-F82528
XRPX Acc No: N2007-692304
Data signals reception method of digital signal processing (DSP) based receiver involves adjusting sampling signals individually to reduce phase errors between received data signal and sampling signal in analog **to** digital converter paths
Patent Assignee: BROADCOM CORP (BROA-N)
Inventor: **AGAZZI O** ; **GOPINATHAN V**
Patent Family (1 patents, 1 countries)
Patent Application
Number Kind Date Number Kind Date Update
US 20070263673 A1 20071115 US 2000219918 P 20000721 200780 B
US 2001273215 P 20010301
US 2001909896 A 20010723
US 200285071 A 20020301
US 2007826414 A 20070716

Priority Applications (no., kind, date): US 2000219918 P 20000721; US 2001273215 P 20010301; US 2001909896 A 20010723; US 200285071 A 20020301; US 2007826414 A 20070716

Patent Details
Number Kind Lan Pg Dwg Filing Notes
US 20070263673 A1 EN 41 18 Related to Provisional US 2000219918
Related to Provisional US 2001273215
C-I-P of application US 2001909896
Continuation of application US 200285071
Continuation of patent US 7245638

...sampling signals individually to reduce phase errors between received data signal and sampling signal in analog **to** digital converter paths
Inventor: **AGAZZI O** ...

... **GOPINATHAN V**

Alerting Abstract ...generating sampling signals having an associated phase with respect to the received data signal (102). **Analog** to **digital converter** (**ADC**) **paths** are controlled with the sampling signals to sample the data signal at the associated phases...
...phase errors between the received data signal and each of the sampling signal in the **ADC** paths, and a digital signal (106) representing the received data signal is produced from the...
...ADVANTAGE - Reduced error in one or more feedback loops to generate equalizer coefficients, to optimize **ADC** sampling phases for timing recovery, and to optimize gain for automatic gain control (AGC...

Original Publication Data by Authority

Argentina

Assignee name & address:
Inventor name & address:
Agazzi, Oscar ...

... **Gopinathan, Venugopal**
Examiner:
Original Abstracts:
...schemes. The present invention is implemented as a multi-path parallel receiver in which an **analog** -to- **digital converter** (" **ADC** ") and/or a digital signal processor ("DSP") are implemented with parallel paths that operate at...

...based receiver in accordance with the invention includes a separate timing recovery loop for each **ADC** path. In an embodiment, a parallel DSP-based receiver includes a separate automatic gain control (AGC) loop for each **ADC** path. In an embodiment, a parallel DSP-based receiver includes a separate offset compensation loop for each **ADC** path. In an embodiment, the present invention is implemented as a multi-channel receiver that...
Claims:
...sampling signals, each of said N sampling signals having an associated phase;(c) controlling N **analog** -to- **digital converter** (" **ADC** ") **paths** with said N sampling signals to sample said data signal at said phases;(d) individually...

...between said received data signal and each of said N sampling signals in said N **ADC** paths; and(e) generating a digital signal representative of said received data signal from samples received from said N **ADC** paths.

^ 14/3,K/2 (Item 2 from file: 350)
DIALOG(R)File 350:Derwent WPIX

0005492216 - Drawing available
WPI ACC NO: 1991-094510/199113
XRPX Acc No: N1991-073019
Communication system analog **-to-** digital converter **- combines M-bit digital signa with N-M digital signal to give N-bit digital signal representing received analog signal**
Patent Assignee: AT & T BELL LAB (AMTT)
Inventor: **AGAZZI O E**
Patent Family (1 patents, 1 countries)

Patent			Application			
Number	Kind	Date	Number	Kind	Date	Update
US 4999830	A	19910312	US 1989412257	A	19890925	199113 B

Priority Applications (no., kind, date): US 1989412257 A 19890925

Communication system analog **-to-** digital converter **-**

Original Titles:
Communication system **analog** -to- **digital converter** using echo information to improve resolution

Inventor: **AGAZZI O E**

Alerting Abstract ...has at least one terminal that simultaneously applies an analog signal corresponding to a first **digital** stream to the **link** and converts an **analog** signal from the **link** into a second digital stream. The analog signal received from the link has a near...

Original Publication Data by Authority

Argentina

Assignee name & address:
Inventor name & address:
Agazzi, Oscar E ...
Examiner:
Original Abstracts:
A communication system for exchanging digital signals over a **transmission link** has at least one terminal that simultaneously applies an analog signal corresponding to a first **digital** stream to the **link** and converts an **analog** signal from the **link** into a second **digital** stream. The analog **signal** received from **the link** has a near end echo component related to the first digital stream. The second digital...
Claims:
?

NPL Full Text Files:-

File 275:Gale Group Computer DB(TM) 1983-2009/Feb 11
(c) 2009 Gale/Cengage
File 47:Gale Group Magazine DB(TM) 1959-2009/Feb 25
(c) 2009 Gale/Cengage
File 621:Gale Group New Prod.Annou.(R) 1985-2009/Jan 30
(c) 2009 Gale/Cengage
File 636:Gale Group Newsletter DB(TM) 1987-2009/Feb 16
(c) 2009 Gale/Cengage
File 148:Gale Group Trade & Industry DB 1976-2009/Feb 20
(c) 2009 Gale/Cengage
File 624:McGraw-Hill Publications 1985-2009/Mar 06
(c) 2009 McGraw-Hill Co. Inc
File 15:ABI/Inform(R) 1971-2009/Mar 07
(c) 2009 ProQuest Info&Learning
File 635:Business Dateline(R) 1985-2009/Mar 09
(c) 2009 ProQuest Info&Learning
File 9:Business & Industry(R) Jul/1994-2009/Mar 06
(c) 2009 Gale/Cengage
File 610:Business Wire 1999-2009/Mar 09
(c) 2009 Business Wire.
File 810:Business Wire 1986-1999/Feb 28
(c) 1999 Business Wire
File 647:UBM COMPUTER FULLTEXT 1988-2009/Mar W1
(c) 2009 UBM, LLC
File 674:Computer News Fulltext 1989-2006/Sep W1
(c) 2006 IDG Communications
File 696:DIALOG Telecom. Newsletters 1995-2009/Mar 06
(c) 2009 Dialog
File 613:PR Newswire 1999-2009/Mar 09
(c) 2009 PR Newswire Association Inc
File 813:PR Newswire 1987-1999/Apr 30
(c) 1999 PR Newswire Association Inc
File 370:Science 1996-1999/Jul W3
(c) 1999 AAAS
File 20:Dialog Global Reporter 1997-2009/Mar 09
(c) 2009 Dialog
File 16:Gale Group PROMT(R) 1990-2009/Feb 16
(c) 2009 Gale/Cengage
File 160:Gale Group PROMT(R) 1972-1989
(c) 1999 The Gale Group
File 75:TGG Management Contents(R) 86-2009/Feb W2
(c) 2009 Gale/Cengage
File 80:TGG Aerospace/Def.Mkts(R) 1982-2009/Feb 12
(c) 2009 Gale/Cengage
File 88:Gale Group Business A.R.T.S. 1976-2009/Mar 06
(c) 2009 Gale/Cengage
File 112:UBM Industry News 1998-2004/Jan 27
(c) 2004 United Business Media
File 141:Readers Guide 1983-2009/Jan
(c) 2009 The HW Wilson Co
File 587:Jane`s Defense&Aerospace 2009/Jan W4
(c) 2009 Jane`s Information Group

Set	Items	Description
S1	169163	DIGITAL(3W)(CHANNEL??? OR PATH??? OR LINK??? OR LINES)
S2	32128	ANALOG(3W)(PATH??? OR LINK??? OR LINES OR CHANNEL??? OR CHANEL???)
S3	127699	ADC OR (ANALOG(2W)DIGITAL OR A()D)(2W)CONVER??????
S4	16080	(PLURAL? OR MANY OR MULTI OR MULTIPLE? ? OR NUMEROUS?? OR SEVERAL? ? OR DIFFERENT?? OR TWO OR ARRAY??)(3N)(S1 OR S2)
S5	2137	(SMALLER OR LOWER OR LESS???)(9N)(S1 OR S2)
S6	2678	(GREATER OR HIGHER OR LARGER OR BIGGER)(9N)(S1 OR S2)
S7	5	AU=(AGAZZI O? OR AGAZZI, O? OR GOPINATHAN V? OR GAPINATHAN, V?)
S8	807	(MATCH???? OR COMPAR????)(5N)(S1 OR S2)
S9	0	S1(S)S2(S)S3(S)S4(S)(S5 OR S6)
S10	3	S1(S)S2(S)S3(S)(S5 OR S6)
S11	3	RD (unique items)
S12	4	S1(50N)S2(50N)S3(50N)(S5 OR S6)
S13	3	RD (unique items)
S14	2	S13 NOT S11
S15	4	S1(S)S2(S)S3(S)S8
S16	2	RD (unique items)
S17	5	S1(50N)S2(50N)S3(50N)S8
S18	3	RD (unique items)
S19	0	S7 AND S1 AND S2 AND S3

11/3,K/1 (Item 1 from file: 275)
DIALOG(R)File 275:Gale Group Computer DB(TM)
(c) 2009 Gale/Cengage. All rts. reserv.

01209784 SUPPLIER NUMBER: 04720204 (USE FORMAT 7 OR 9 FOR FULL TEXT)
Implementing a video-teleconferencing system need not be as complex as you think.
Daly, Ed
Communications News, v24, p35(2)
Feb, 1987
LANGUAGE: ENGLISH RECORD TYPE: FULLTEXT
WORD COUNT: 1578 LINE COUNT: 00129

... video presentation and to minimize user discomfort.
Most organizations connect their video-teleconference sites with **digital channels**. More-readily available and **less** expensive than **analog channels**, **digital channels** can be terrestrial or satellite and may be accessed on a full-time or part-time basis. A video codec provides the **analog / digital conversion** and digital compression that enables the use of US **digital channels** at 1.544 Mb/s, 768 kb/s or even 56 kb/s. (European channels...

11/3,K/2 (Item 1 from file: 674)
DIALOG(R)File 674:Computer News Fulltext
(c) 2006 IDG Communications. All rts. reserv.

067805
V.90 promises smooth high-speed modem move
Fast Modems gain ally in spec that maximizes the digital aspect of the phone network.
Byline: Chris Brock
Journal: Network World Page Number: 35
Publication Date: July 27, 1998
Word Count: 740 Line Count: 69

Text:
... V.90 technology lets modems receive data at up to 56K bit/sec, even over **analog** phone **lines**, by exploiting the fact that most ISPs' access servers are connected to digital circuits at...

... limiting factor in the speed of data transmission because of the inherent noise it contributes. **Digital lines** still have noise, but they have **less** noise and a higher ceiling. Fortunately, most telephone networks throughout the world are digital. So...

... employ one bidirectional channel for sending and receiving. The receiving portion of the V.90 **analog** modem's **channel** is capable of **higher** speeds because no information is lost in the digital-to-analog conversion. However, the sending portion of the channel goes through an **analog** -to- **digital conversion**, which can limit data transmission to 28.8K bit/sec speeds.Because the path from...

11/3,K/3 (Item 1 from file: 696)

0000959177
Digital Transmission, Part 1: Carrier-to-Noise Ratio, Signal-to-Noise Rati o and\Modulation Error Ratio
Communications Technology
June 15, 2007 DOCUMENT TYPE: NEWSLETTER
PUBLISHER: PHILLIPS BUSINESS INFORMATION
LANGUAGE: ENGLISH WORD COUNT: 8664 RECORD TYPE: FULLTEXT

TEXT:
...generally accepted to be a predetection
measurement - that is, one made at RF. When only **analog** TV **channels**
were carried
on cable networks, CNR was understood to be the difference, in decibels,
between...

...MHz band centered within the cable television channel." This latter
definition
is applicable only to **analog** NTSC TV **channel** CNR measurements and
defines the
approximate bandwidth of the baseband video that modulates the channel...

...rules mandate a minimum CNR of 43 dB,
good engineering practice targets end-of-line **analog** TV **channel** CNR in
the 46 to
49 dB range. More on this topic later.

Analog video...

...states an assumed
minimum 35 dB CNR for downstream digitally modulated signals. If the
network
analog TV **channel** CNR is maintained in the 46 dB or **higher** range, in
most cases,
there will be little or no problem complying with the DOCSIS...

...C" in CNR - is
the average power level of the digitally modulated signal, often called
digital
channel power. It is measured in the full occupied bandwidth of the
signal; for
example, 6...by analog and digital front-end
components that perform tuning, automatic gain control, channel selection,
analog -to- **digital** **conversion** , and related functions. The square-root
Nyquist
filter has a response "matched" to the symbol...

...downstream
end-of-line CNR of 46 dB with +15 dBmV subscriber tap levels for **analog**
TV
channels , and a downstream 64-QAM DOCSIS digitally modulated signal is
carried

at -10 dBc. Thus, the **digital channel** power of the 64-QAM signal at the tap
spigot will be +5 dBmV, or 10 dB **lower** than the +15 dBmV **analog** TV **channel**
levels. What is the 64-QAM signal CNR? It is not 36 dB as one might first assume.
Because **analog** TV **channel** CNR is 46 dB at the tap spigot, the noise-floor
amplitude NNTSC for the **analog channels** is +15 dBmV - 46 dB = -31 dBmV (4 MHz
noise power bandwidth for **analog** NTSC TV **channels**). To determine the 64-QAM
signal CNR, we have to first calculate what the noise...

...AWGN through to the demodulator.

Upstream Digitally Modulated Signal CNR-an Example

Assume that the **digital channel** power of a 3.2 MHz bandwidth 16-QAM signal at the CMTS upstream port...front end: Analog and digital front-end components
perform tuning, automatic gain control, channel selection, **analog** -to-**digital**
conversion , etc. Their purpose is to preprocess the signal so that the individual QAM RF channels...

14/3,K/1 (Item 1 from file: 47)
DIALOG(R)File 47:Gale Group Magazine DB(TM)
(c) 2009 Gale/Cengage. All rts. reserv.

05148005 SUPPLIER NUMBER: 20503930 (USE FORMAT 7 OR 9 FOR FULL TEXT)
Speed demons: testing the fastest modems you can buy - 12 of them.(56Kbps modems)(Cover Story)(Evaluation)
Gaffney, John
Popular Mechanics, v175, n5, p72(6)
May, 1998
DOCUMENT TYPE: Cover Story Evaluation ISSN: 0032-4558 LANGUAGE: English RECORD TYPE: Fulltext; Abstract
WORD COUNT: 2300 LINE COUNT: 00222

... SportsZone and hit ENTER. Your modem then connects to the ISP with your request, through **analog** phone **lines** . Your ability to upload, therefore, is limited to the phone line's analog limit of...

...ISP. The signal then comes back to your modem as an analog signal. This asymmetrical **analog** -to- **digital** -to-analog **conversion** happens for 85% of PC users' homes. If lines are multiplexed in your area, 33...

...system. 3Com offers a phone line analysis at x2.usr.com/linetest1.html. Again, until **analog** phone **lines** become equipped with **higher** bandwidth, downloading with a typical modem isn't going to be the quickest thing around...

...data rather than using analog modulation. 3Com claims that its x2 protocol actually widens the **digital** return **path** , and therefore enables the x2 products to grab more available bandwidth. Bottom line: The technological...

14/3,K/2 (Item 1 from file: 15)
DIALOG(R)File 15:ABI/Inform(R)
(c) 2009 ProQuest Info&Learning. All rts. reserv.

01674351 03-25341
V.90 promises smooth high-speed modem move
Brock, Chris
Network World v15n30 PP: 35 Jul 27, 1998
ISSN: 0887-7661 JRNL CODE: NWW
WORD COUNT: 771

...TEXT: V.90 technology lets modems receive data at up to 56K bit/sec, even over **analog** phone **lines** , by exploiting the fact that most ISPs' access servers are connected to digital circuits at...

...limiting factor in the speed of data transmission because of the inherent noise it contributes. **Digital lines** still have noise, but they have **less** noise and a higher ceiling. Fortunately, most telephone networks throughout the world are digital. So...

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Because the path from...

16/3,K/1 (Item 1 from file: 275)
DIALOG(R)File 275:Gale Group Computer DB(TM)

01204956 SUPPLIER NUMBER: 06334247 (USE FORMAT 7 OR 9 FOR FULL TEXT)
Best of 1987: analog & power. (Electronic Design Top 100 1987) (directory)
Electronic Design, v35, n30, p29(7)
Dec 23, 1987
DOCUMENT TYPE: directory ISSN: 0013-4872 LANGUAGE: ENGLISH
RECORD TYPE: FULLTEXT
WORD COUNT: 7615 LINE COUNT: 00576

... skew between them. Nowhere is this more difficult than in the area of parallel comparisons-- **matching** signals on parallel **analog** or **digital lines** . Comparators go to work in many applications, from simple crossover detectors to flash **a - d converters** .
Now for the first time designers can compare such signals, in clocked mode in about...

16/3,K/2 (Item 2 from file: 275)
DIALOG(R)File 275:Gale Group Computer DB(TM)

01204418 SUPPLIER NUMBER: 04729599 (USE FORMAT 7 OR 9 FOR FULL TEXT)
Octal comparator gives superfast performance.
Weiss, Ray
Electronic Design, v35, p41(2)
March 5, 1987
ISSN: 0013-4872 LANGUAGE: ENGLISH RECORD TYPE: FULLTEXT
WORD COUNT: 988 LINE COUNT: 00075

TEXT:
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18/3,K/1 (Item 1 from file: 275)
DIALOG(R)File 275:Gale Group Computer DB(TM)

01204956 SUPPLIER NUMBER: 06334247 (USE FORMAT 7 OR 9 FOR FULL TEXT)
Best of 1987: analog & power. (Electronic Design Top 100 1987) (directory)
Electronic Design, v35, n30, p29(7)
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18/3,K/2 (Item 2 from file: 275)
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01204418 SUPPLIER NUMBER: 04729599 (USE FORMAT 7 OR 9 FOR FULL TEXT)
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TEXT:
...by minimizing skew. Nowhere is this more difficult than in the area of parallel comparisons-- **matching** signals on parallel **analog** or **digital lines** . Comparators go to work in many applications, from simple crossover detectors to digital-to-analog and flash **a - d converters** .

18/3,K/3 (Item 1 from file: 88)
DIALOG(R)File 88:Gale Group Business A.R.T.S.

07192727 SUPPLIER NUMBER: 132679444
Hybrid (SIGMA)(DELTA) modulators with adaptive calibration.(Author Abstract)
Shim, Jae Hoon; Park, In-Cheol; Kim, Beomsup
IEEE Transactions on Circuits and Systems-I-Regular Papers, 52, 5, 885(9)
May, 2005
DOCUMENT TYPE: Author Abstract LANGUAGE: English RECORD TYPE: Abstract

...AUTHOR ABSTRACT: high-order (SIGMA)(DELTA) modulator stable. However, the hybrid (SIGMA)(DELTA) modulator relies on precise **matching** of **analog** and **digital paths** . In this paper, a calibration technique to alleviate

possible mismatch between **analog** and **digital paths** is proposed. The calibration adaptively adjusts the digital integrators so that their transfer functions match...

...modulators, the calibration technique is verified.

Index Terms--Adaptive signal processing, calibration, (SIGMA)(DELTA) modulation, **analog - digital conversion** .